1968

Radiation and annealing characteristics in neutron bombarded transistors operated in the inverse configuration

Lo-Soun Su

Department:

RADIATION AND ANNEALING CHARACTERISTICS IN NEUTRON BOMBARDED TRANSISTORS OPERATED IN THE INVERSE CONFIGURATION

BY

LO-SOUN SU, 1942

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THESIS

submitted to the faculty of

THE UNIVERSITY OF MISSOURI - ROLLA

in partial fulfillment of the requirements for the

Degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

Rolla, Missouri

1968

Approved by

Charles A. Lober (advisor) Albert E. Slaven

Norman Dillman

ABSTRACT

When operating a silicon planar epitaxial transistor in the inverse configuration (i.e., with the emitter functioning as a collector and the collector functioning as an emitter) the bulk space-charge volume of the new "emitter-base" junction is increased by a factor of 26.5 times that of the normal emitter-base junction. The carrier concentration in the new "emitter" is decreased by five orders of magnitude from that of the normal emitter, thus making it easier to investigate the effects of neutron radiation on the space-charge region and at the surface.

Experiments using biasing of the new "emitter-base" junction during neutron radiation to change the depletion layer width have been performed. Surface effects in the form of an inversion layer adjacent to the "emitter-base" junction have been observed. These surface effects cause the base current to increase by a factor of 5 to 10 in the low "emitter-base" voltage region and the "emitter-base" junction capacitance to increase by a factor of approximately 2 at a fluence level of 2×10^{14} nvt. The "emitter-base" junction was reverse biased at 3.0V during irradiation in this experiment. These surface effects were found to significantly anneal at room temperature.

A decrease in the diffusion potential of the "emitter-base" junction was predicted on theoretical grounds and experimentally observed after irradiation. The diffusion potential increased after isochronal annealing but did not

return to its pre-irradiated value.

For the annealing studies, pairs of devices with nearly identical characteristics (matched within 10 per cent) were used with one device of each pair used for isothermal annealing and the other device of each pair used for isochronal annealing. One pair of devices was forward biased at 0.5V, the second pair of devices was reverse biased at 3.0V, and the third pair of devices was unbiased during isothermal and isochronal annealing. Activation energies of 0.19 ± 0.04eV and 0.86 ± 0.15eV in the bulk space-charge region, 0.34 ± 0.06eV and 0.98 ± 0.18eV in the neutral base region were calculated from these isochronal and isothermal annealing data. No solid conclusions concerning the annealing rate of defects in the bulk space-charge region can be drawn because of the apparent descrepencies between the isothermal and isochronal annealing data. The unannealed fraction of defects in the neutral base region was found to increase in the temperature range from 50° to 100°C and was attributed to an increase in the concentration of A-centers (oxygen-complexes).

The annealing rates of defects both in the space-charge region and in the neutral base region were enhanced by the externally applied reverse voltage over temperature range from 150°C to 180°C, while the annealing rate of defects in the p-type neutral base region was retarded by the minority carrier injection above 50°C. This result agrees with previous results of Sander and Gregory.

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I. INTRODUCTION

An anomalous neutron-induced base current component has been identified and found to vary with emitter-base voltage as[1,2,3,4]

$$I_{B_{INC}} = K_V \cdot X_m(V_{BE}) \cdot A_E \cdot \phi \cdot \exp\left(\frac{qV_{BE}}{nkT}\right), \quad (1\text{-}1)$$

where A_E = effective emitter area (cm^2),

K_V = volume damage constant (amperes/cm^3/nvt),

$X_m(V_{BE})$ = depletion layer width (cm),

ϕ = neutron fluence (neutrons/cm^2),

$n \simeq 1.5$.

This neutron-induced base current increases in proportion to the neutron fluence as indicated by equation (1-1). It was found to dominate the transistor current gain over a wide range of current levels and be primarily responsible for the degradation of current gain at low and intermediate current levels through degradation of the emitter efficiency.

Anomalous annealing phenomena which have also been studied previously[1,2,3] indicate that the neutron-induced defects in the emitter-base space-charge region of a transistor anneal differently from defects in the neutral base region. A slight field dependence of the annealing of neutron-induced defects was observed recently but appeared to be quite complex[5].

Impurity profiles[6] of 2N914 transistors indicate that the depletion layer width of the collector-base junction is about 5 times wider than that of the emitter-base junction. The effective area of the collector-base junction is 5.39

times that of the emitter-base junction.

Thus, if the roles of the collector and emitter are interchanged (that is, if the normal emitter is operated as a "collector" and the normal collector is operated as an "emitter") the effective volume of the new "emitter-base" junction is about 27 times that of the normal emitter-base junction. From equation (1-1), $I_{B_{INC}}$ should increase by a factor of about 27 if the device is operated under the same conditions as in the normal configuration. Therefore, the behavior of the neutron-induced base current which originates in the bulk space-charge region can be determined more accurately in the low current region below the onset of voltage deviation (emission crowding).

Surface effects can be a very important factor in semiconductor devices. Since the collector-base junction is reverse biased in the normal operating configuration, reverse biasing this ("emitter-base") junction during neutron radiation will indicate whether surface effects can occur at the collector-base junction during normal operation in a neutron radiation environment. Since the carrier concentration in the emitter of a 2N914 transistor is about 10^5 times that of the collector, the Fermi level in the emitter region lies closer to the conduction band than does the Fermi level in the collector region. Thus, inversion layers are more easily formed in the "emitter-base" junction region. This allows the study of neutron radiation-induced surface effects by using devices having identical characteristics but biased at

different junction voltages.

A computer program using a least-squares fitting technique can be used to estimate the value of the diffusion potential by using the measured data of junction capacitance versus externally applied voltage[6,7]. This permits the study of the radiation and annealing characteristics of the diffusion potential in neutron bombarded transistors.

The activation energy[8] which characterizes the recovery of the defects can be calculated by combining the data from both isothermal and isochronal annealing of two identical devices. It is thought that neutron radiation introduces many defect levels[9] which are distributed throughout the forbidden energy band with some dominating the characterics. In order to determine the effect of different biasing voltages on the activation energy in a certain temperature range, three sets of paired devices can be annealed, with each pair annealed at a different junction bias voltage. One device of each pair can be used for isothermal annealing and the other device of each pair can be used for isochronal annealing. This also allows one to study the field dependence of the annealing rate of neutron-induced defects in both the bulk space-charge region and the neutral base region.

II. NEUTRON-INDUCED SURFACE EFFECTS

Impurity profiles[6] of 2N914 transistors indicate that the majority carrier concentration of the normal emitter is about 1.67×10^5 times that of the "emitter" as used in this work. Therefore, the Fermi level in the "collector" region lies closer to the conduction region than the Fermi level in the "emitter" region and inversion layers are more easily formed on the "emitter". Furthermore, the carrier concentration in the base is about 10 times that of the "emitter"; thus, the probability of forming an inversion layer at the "emitter" surface is larger than that at the base surface.

The environment within 2N914 (npn) transistor cans and also those of the devices used in this work is nitrogen gas, which can be ionized by neutron radiation. The reverse biased "emitter-base" junction voltage induces a strong field across the junction which either attracts negatively charged ions to the "emitter" or attracts positively charged ions to the base. Charge neutrality is then achieved by the attraction of oppositely charged carriers from the semiconductor bulk. If the doping concentration of the "emitter" or the base is sufficiently low, an inversion layer is formed in spite of the oxide passivation.

This neutron-induced inversion layer increases the "emitter-base" junction area and causes an increase in junction capacitance. If positively charged ions are attached to the base surface, an inversion layer will form on the base side of the "emitter-base" junction. The maximum width which

the junction can extend into the base side is 20μ because it cannot extend across the metal contact shown by cross-hatching in Figure 1 (which shows the geometric structure of the transistors used in this work). Thus, the maximum increment of junction area due to extension of the junction into the base region would be:

$$\Delta A = \pi[(115)^2 - (95)^2] \times 10^{-8} cm^2. \qquad (2\text{-}1)$$

Since the junction capacitance is given by the expression:

$$C = \frac{\varepsilon A}{X} , \qquad (2\text{-}2)$$

where ε is the permittivity of the material, A is the effective "emitter-base" junction area, X is the depletion layer width. Because the total number of defects introduced at the fluences used in this surface effects study ($\phi < 2 \times 10^{14}$ nvt) is much smaller than the silicon atom concentration, the permittivity was assumed to be constant. The total junction capacitance after the extension of junction in the base side would be:

$$C + \Delta C = \frac{\varepsilon A}{X} + \frac{\varepsilon \Delta A}{X_1} , \qquad (2\text{-}3)$$

where X_1 is the thickness of the neutron-induced surface channel. Since the value of X_1 is not known, one may make a rough calculation by assuming that X and X_1 are of the same order of magnitude. The total junction capacitance possible after extension of the junction into the base side could be

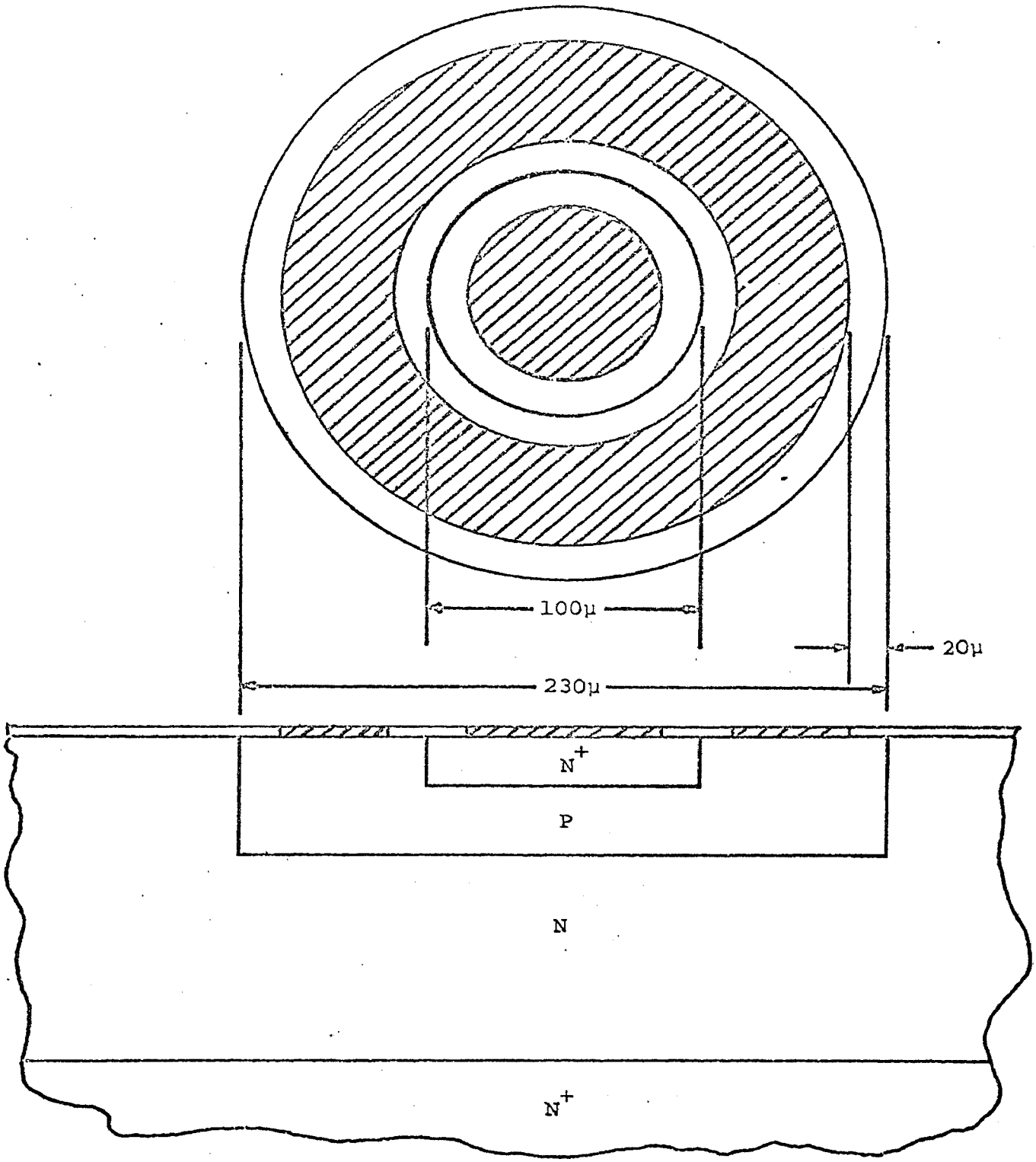


Figure 1. Geometric structure of planar epitaxial transistors used in this work.

expressed as:

$$C + \Delta C = \frac{\varepsilon (A + \Delta A)}{X}. \qquad (2\text{-}4)$$

Therefore, at each fluence level the ratio of the junction capacitances with and without the extension of junction into the base side only would be:

$$\frac{C + \Delta C}{C} = \frac{A + \Delta A}{A} = 2 - \left(\frac{95}{115}\right)^2 = 1.318. \qquad (2\text{-}5)$$

Thus, if the "emitter-base" junction capacitance should increase by more than 31.8 per cent of the original value, it can be concluded that the inversion layer was formed on the "emitter" side rather than the base side, of the "emitter-base" junction, or on both sides.

An additional surface recombination current is produced by the neutron-induced inversion layer. The surface recombination current is small and causes an effective increase in base current only in the low "base-emitter" voltage region. At higher "base-emitter" voltages, the bulk recombination current is considerably larger than the surface recombination current and the bulk recombination current dominates in this range.

The density of the interface states is usally much smaller than that of the layer states, but it is postulated[10] that interface states have capture probabilities many orders of magnitude greater than layer states. Therefore, any observed recombination of the carriers at the

surface can be attributed mainly to recombination at the interface The interface states were found to be independent of ambient conditions but apparently reflect the quality of the initial surface treatment[10]. Since the effective lifetime is affected by surface and bulk recombination and the surface recombination velocity depends largely on the initial surface treatment, the effective lifetime should not be largely affected by a neutron-induced inversion layer if the inversion layer were caused by the attraction to and entrapment on the silicon dioxide layer of negatively charged nitrogen atoms.

Four devices, plus one set of three devices with indentical characteristics, were irradiated in nine steps to a neutron fluence of 2×10^{14}nvt. In the set of three devices, one was reverse biased at 3.0V, the second was forward biased at 0.5V while the third device was unbiased during irradiation. The remaining four devices were unbiased during irradiation. All the bias voltages were applied to the "emitter-base" junction.

The devices used in this radiation effects study were obtained from Texas Instruments. The devices were fabricated from a single wafer with impurity profiles and junction depths identical to that of the 2N914 transistor. However, these devices differed from the 2N914 in that they were not gold doped. The devices were designated as SA7472 transistor by the manufacturer.

All device irradiations were made simultaneously in the

University of Missouri-Rolla Research Reactor to insure equal fluences upon exposure. The transistors were irradiated in an aluminum sample holder containing boron carbide to shield the devices from thermal neutrons. This allows one to consider only the effects of fast neutrons (E > 10keV).

"Emitter-base" junction capacitance C_{BE}, minority carrier lifetime at the "emitter-base" junction τ_{BE} and at the "collector-base" junction τ_{BC} were measured. Current-voltage characteristics were plotted at each irradiation step.

The "emitter-base" junction capacitance (C_{BE}) of devices biased at different voltages during irradiation (measured at an externally applied junction voltage of V_{BE} equal 0.0V) versus neutron fluence is shown in Figure 2. As can be seen in Figure 2, C_{BE} increases with neutron fluence. The "emitter-base" junction capacitance of the device forward biased at 0.5V and of the unbiased devices has only a slight increase (less than 5%) after neutron irradiation. But the "emitter-base" junction capacitance of the device reverse biased at 3.0V during irradiation increased very rapidly with neutron fluence. At a fluence of 6×10^{13}nvt and higher, C_{BE} increases less and less rapidly and tends to approach some constant value approximately 2 times larger than the pre-irradiated value.

The base current-voltage characteristics with neutron fluence as a parameter (for the device reverse biased at 3.0V during irradiation) are shown in Figure 3. At the

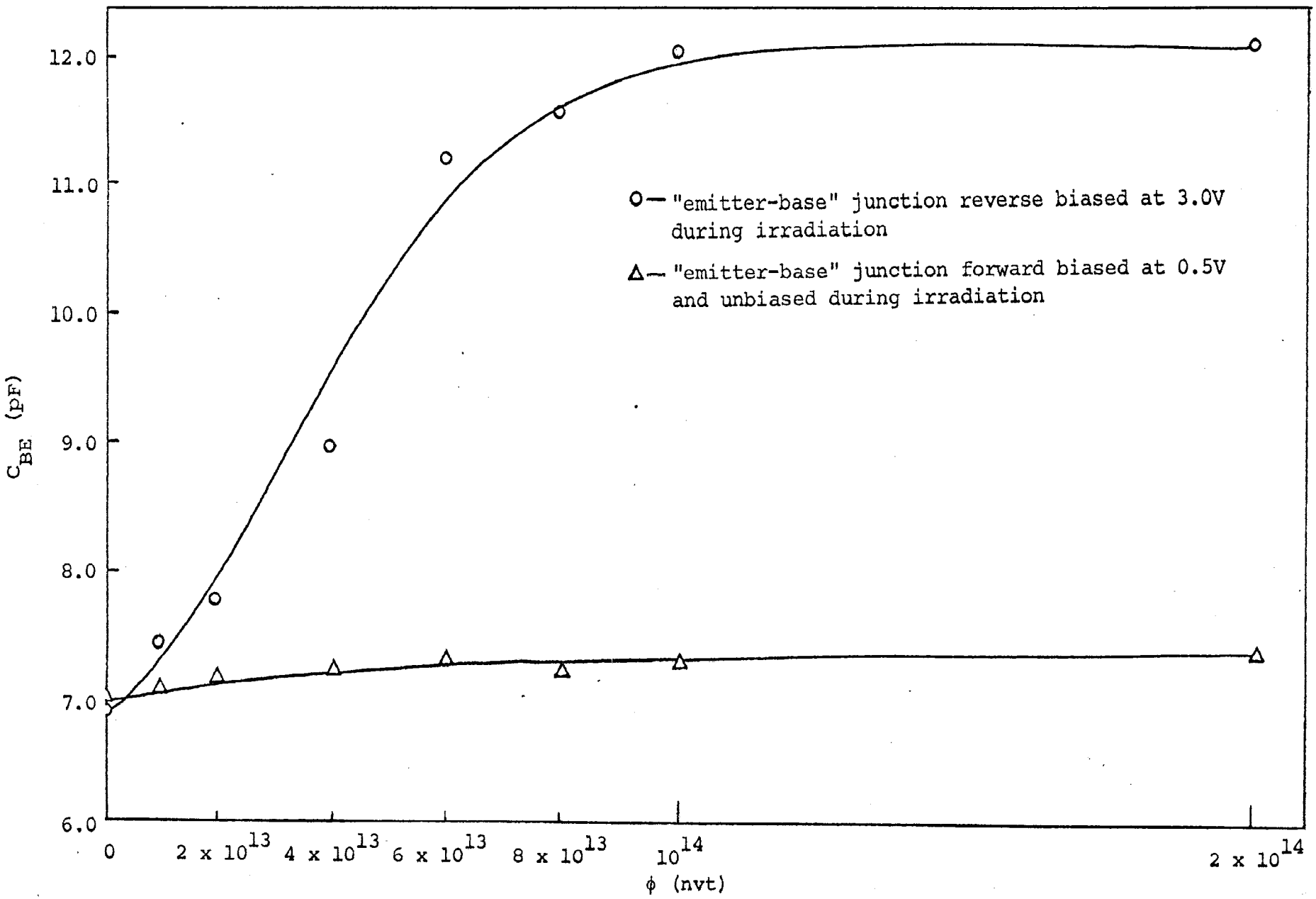


Figure 2. "Emitter-base" junction capacitance versus neutron fluence (measured at 0.0V dc).

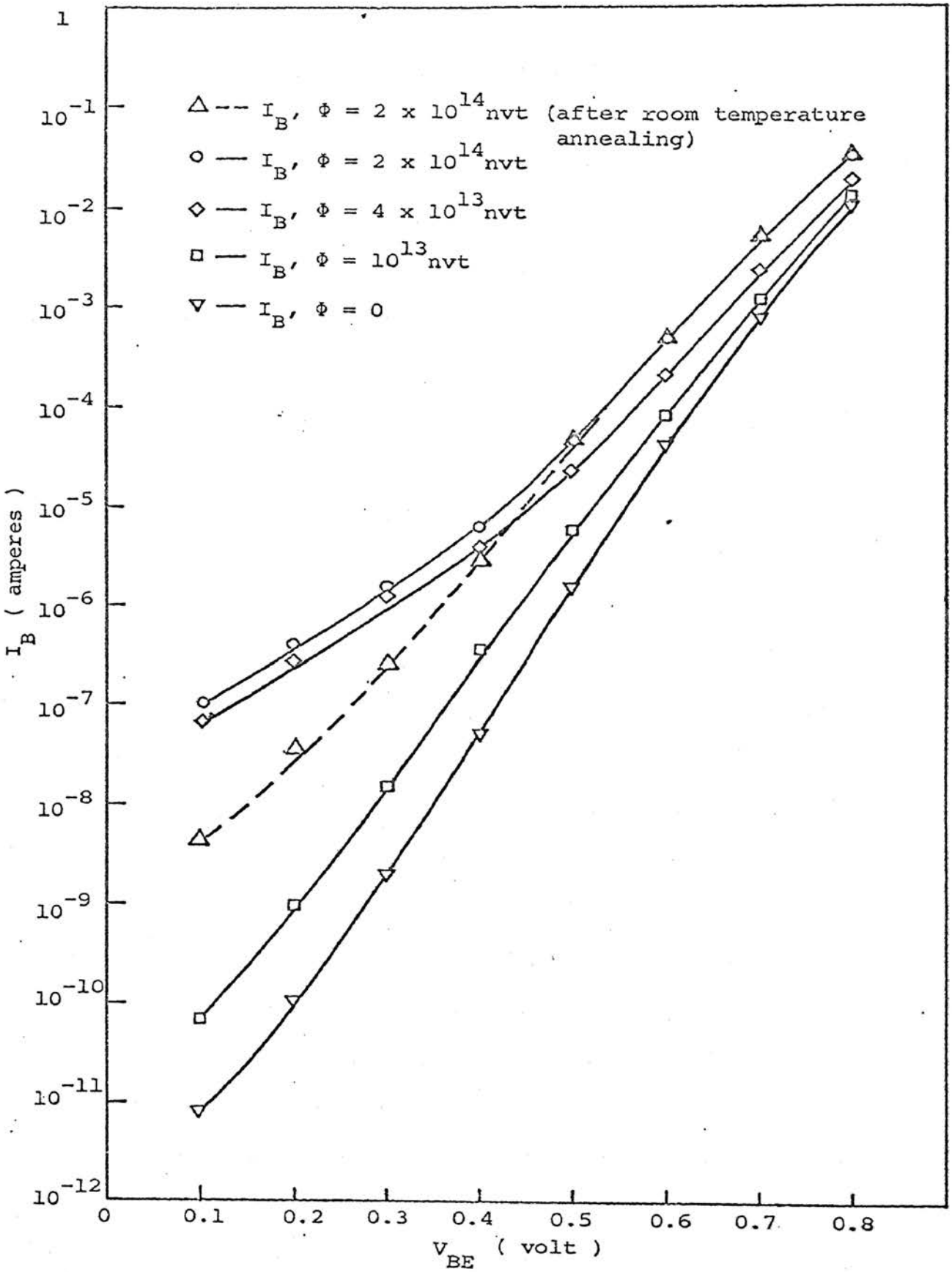


Figure 3. I_B - V_{BE} characteristics for the device reverse biased at 3.0V during irradiation.

fourth ($\phi_4 = 2 \times 10^{13}$nvt) and the fifth ($\phi_5 = 4 \times 10^{13}$nvt) irradiations, a base current component with reciprocal slope terms of n ≃ 2 and 2.8, respectively, has appeared in the low-voltage region. Typical I-V characteristics of base current with neutron fluence as a parameter of the other devices are shown in Figure 4. No large increase of I_B in the low voltage range appeared in any other device. From the previous discussion and the experimental data of C_{BE} - V_{BE} and I_B - V_{BE} characteristics, it is evident that neutron-induced negatively charged nitrogen ions have formed an inversion layer on the "emitter" surface. The increase in base current component with reciprocal slope terms of n ≃ 2.0 and 2.8 is due to the formation of an inversion layer. Figure 3 shows that a large fraction of this particular current component increase anneals at room temperature in approximately four weeks.

Figure 5 is a table of τ_{BE} versus neutron fluence for seven devices. It should be noted that while τ_{BE} decreases with neutron fluence, it is not a function of junction voltage during irradiation. While the inversion layer is formed for the device reverse biased at 3.0V during irradiation, it may be noted from these data that the neutron-induced inversion layer does not appreciably affect the minority carrier lifetime. From this one may conclude that the inversion layer is caused by the entrapment of nitrogen ions on the oxide layer.

The reverse bias on the "emitter-base" junction of 3.0V

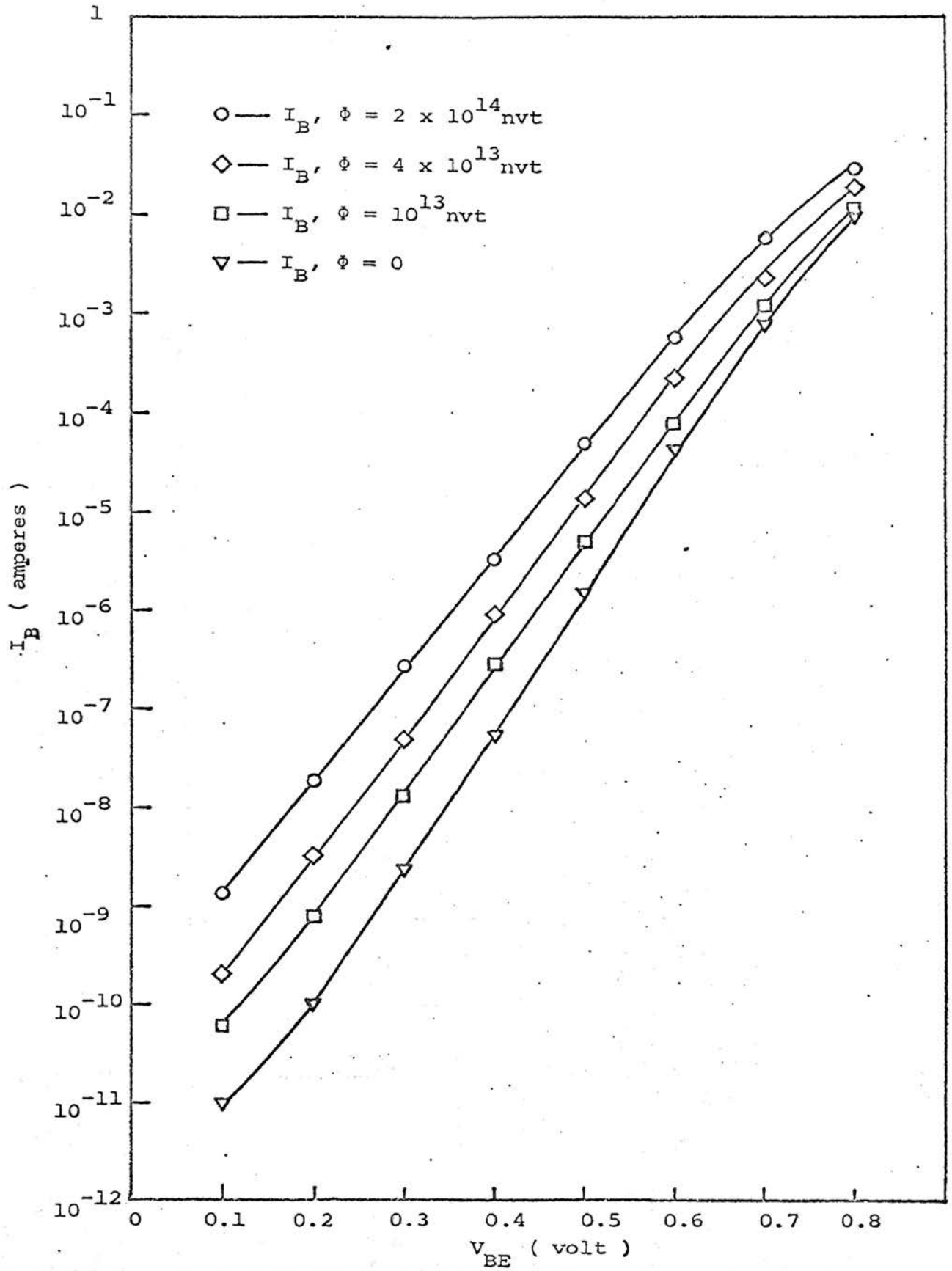


Figure 4. Typical curves of I_B - V_{BE} characteristics for the device forward biased at 0.5V and the unbiased devices during irradiation.

bias voltage during irradiation	+0.5V	-3.0V	0.0V	0.0V	0.0V	0.0V	0.0V
ϕ (nvt) \ device no.	#13	#65	#96	#59	#63	#28	#62
$\phi = 0$	130	130	130	208	208	208	208
$\phi = 10^{13}$	104	83.2	87	104	104	104	104
$\phi = 2 \times 10^{13}$	59.4	69.3	69.6	78	78	78	78
$\phi = 4 \times 10^{13}$	39	34.7	34.7	41.6	41.6	41.6	43.3
$\phi = 6 \times 10^{13}$	26	26	26	26	26	26	26
$\phi = 8 \times 10^{13}$	26	20.8	19.5	20	20.8	20.8	20.8
$\phi = 10^{14}$	*	*	*	*	*	*	*

#13, #65 and #96 are triplicate devices
#59, #63 and #28, #62 are pairs of devices
#13 was forward biased at 0.5V during irradiation
#65 was reverse biased at 3.0V during irradiation
#96, #59, #63, #28 and #64 were unbiased during irradiation
* beyond the limit of measurement

Figure 5. Table of τ_{BE} (ns) versus neutron fluence.

during irradiation was used on other devices, and the same phenomena were found.

Surface effects due to neutron radiation have been thought previously to be negligible[11]. This experiment shows that an inversion layer is formed at the transistor surface near a junction if the doping concentration is low and if the junction is reverse biased during irradiation for devices mounted in gas-filled cans.

III. RADIATION AND ANNEALING CHARACTERISTICS OF THE DIFFUSION POTENTIAL (V_T)

The diffusion potential, V_T, for nondegenerate material at thermal equilibrium is given by equation (3-1)[10].

$$V_T = \frac{kT}{q} \cdot \ln \frac{N_D \cdot N_A}{n_i^2}, \tag{3-1}$$

where N_D = electron concentration in a n-type semiconductor,

N_A = hole concentration in a p-type semiconductor,

n_i = intrinsic carrier concentration,

k = Boltzmann's constant (8.63×10^{-5} eV/°K),

T = absolute temperature in degrees Kelvin,

q = charge of electron (1.6×10^{-19} coulomb).

The dependence of hole and electron concentrations on neutron fluence are given by the following empirical expressions:

$$N_D = N_{D_o} \cdot \exp(-\phi/k_p), \tag{3-2}$$

$$N_A = N_{A_o} \cdot \exp(-\phi/k_n), \tag{3-3}$$

where N_{D_o} and N_{A_o} are the initial carrier concentrations and k_p and k_n are the concentration damage constants for holes and electrons, respectively.

Substituting equations (3-2) and (3-3) into (3-1), one obtains:

$$V_T = \frac{kT}{q}\left(\ln\frac{N_{D_o} \cdot N_{A_o}}{n_i^2} - \frac{\phi}{k_T}\right), \qquad (3\text{-}4)$$

where,

$$\frac{1}{k_T} = \frac{1}{k_p} + \frac{1}{k_n}.$$

Because the effective densities of quantum states in the valence band and in the conduction band (N_V and N_C, respectively) are much larger than the total number of defects introduced at the fluences used in this diffusion potential study (up to 5 x 10^{14}nvt), the intrinsic carrier concentration n_i was assumed to be constant. The diffusion potential may be written as:

$$V_T = \frac{kT}{q}\left(C_1 - \frac{\phi}{k_T}\right), \qquad (3\text{-}5)$$

where,

$$C_1 = \ln\frac{N_{D_o} \cdot N_{A_o}}{n_i^2}.$$

Therefore, the diffusion potential, V_T, should decrease after neutron radiation.

Two methods were used to find the diffusion potential. The first method was to measure the "emitter-base" junction capacitance using a Micro Instrument 1201DS Digital Capacitance Tester. The depletion layer width of a p-n junction decreases with externally applied forward voltage.

If currents and I-R drops were neglected and the applied voltage were increased to the diffusion potential, V_T, the depletion layer width would decrease to zero, and the junction capacitance would tend to infinity. The externally applied voltage which caused C_{BE} to approach infinity (off scale reading i.e., greater than 100pF, on the Capacitance Tester) was assumed to be the diffusion potential. The second method was to estimate V_T using the equation for junction capacitance for nondegenerate material at thermal equilibrium which is generally expressed as[12]:

$$C = \frac{K}{(-V + V_T)^m} , \qquad (3\text{-}6)$$

where V_T = diffusion potential,

V = externally applied junction voltage,

K = a constant,

m = a constant which is between $\frac{1}{2}$ and $\frac{1}{3}$.

A computer program using the least-squares fitting technique was used to estimate the value of V_T by using the measured data of the junction capacitance versus the externally applied voltage. The capacitance values used were measured at forward and reverse biased voltages near zero.

The diffusion capacitance increases as the externally applied forward voltage is increased, thus increasing the capacitance reading and giving a smaller value for V_T than the true value. The value of V_T which was estimated by the computer program using the least-squares fitting technique

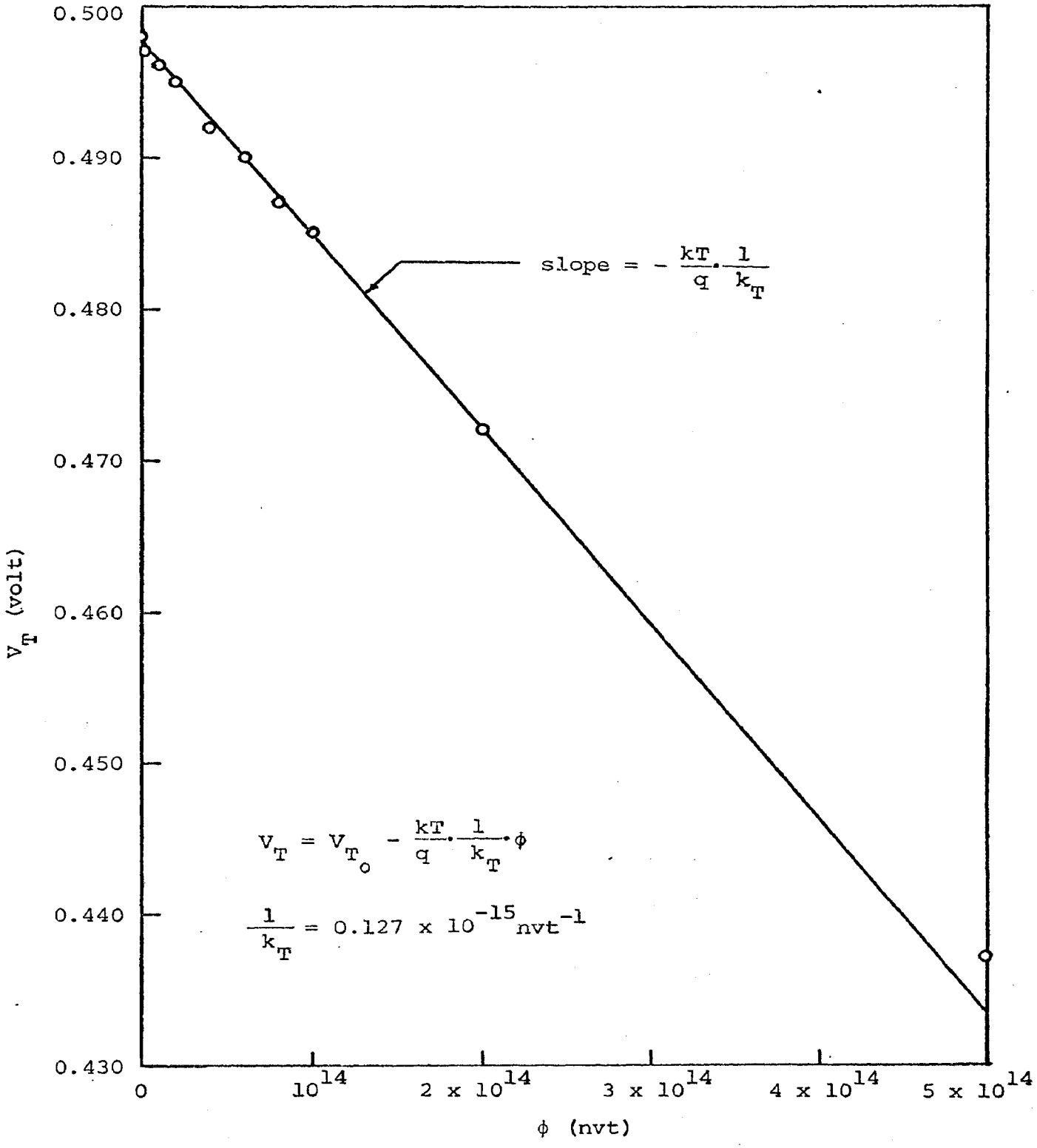


Figure 6. Diffusion potential (V_T) versus neutron fluence.

was used in the calculation, since this method was felt to yield a more accurate value of V_T than that obtained using the off scale reading of the Digital Capacitance Tester.

The diffusion potential, V_T, of the devices was estimated using the least-squares fitting technique at every fluence after neutron radiation. The curves depicting the diffusion potential as function of neutron fluence are illustrated in Figure 6 and show that V_T decreases after neutron irradiation. No effect of the change of V_T on the externally applied bias voltage during irradiation was observed. This is attributed to the increased I-R drop.

The diffusion potential was also estimated using the same least-squares fitting technique after certain isochronal annealing runs. A table of the diffusion potential (normalized to its pre-irradiation value) versus isochronal annealing temperature is illustrated in Figure 7. It was observed that V_T increased after isochronal annealing but that it did not return to its pre-irradiation value.

Temperature (°C)	27	75	95	155	255
Normalized V_T (%)	89.15	89.35	89.95	90.76	91.56

Figure 7. Table of V_T (normalized to its pre-irradiation value) versus annealing temperature.

These experimental results show that the diffusion potential of the "emitter-base" junction decreased to

approximately 90% of its pre-irradiation value at a neutron fluence of 5×10^{14}nvt. The diffusion potential increased after the isochronal annealing but did not anneal completely to its pre-irradiation value.

IV. DEPENDENCE OF ANNEALING RATE ON VOLTAGES APPLIED EXTERNALLY TO THE "EMITTER-BASE" JUNCTION DURING ANNEALING

Three pairs of devices with nearly identical characteristics (matched to within 10 per cent) were irradiated to a fluence of 5×10^{14}nvt. The changes in the characteristics of each pair of devices were nearly identical after neutron radiation. One device of each pair was annealed isochronally and the other device of each pair was annealed isothermally. During the annealing, the "emitter-base" junction of one pair of devices was forward biased at 0.5V, that of the second pair of devices was reverse biased at 3.0V while that of the third pair of devices was unbiased. The "collector-base" junction was open circuited during the annealing. After each annealing run, current-voltage characteristics of each device were measured in the inverse operating configuration. This was done on the Automatic Data Acquisition System of the Space Sciences Research Center[12].

In order to insure accurately known annealing times, the time required to stabilize the device at the annealing temperature and the time required to cool the device out of the annealing range at the end of the annealing run were kept small compared to the total annealing run time. This was accomplished by inserting and withdrawing the device very quickly from a constant high temperature oil bath and cooling the device in a room temperature alcohol bath. An aluminum container for the oil bath was fabricated and

special oils (poymethyl phenyl silicone fluids) were used. Two types of oil were used in order to cover the required annealing temperature range without decomposing the oil. For isochronal annealing the devices were annealed for 20 minute periods at temperatures between 35°C and 295°C in 10°C intervals. Figures 8 and 9 are plots of the unannealed fraction of defects in the bulk space-charge region and in the neutral base region, respectively, versus temperature with the externally applied voltage as a parameter. The values of I_B and I_C were taken at V_{BE} = 500mV. The lines connecting the data points on the annealing characteristic curves in Figures 8 and 9 are for convenience and not meant to portray the annealing characteristics of the defects between the experimental data points.

The first temperature chosen for isothermal annealing was 50°C. The devices were annealed until the recovery rate of defects in both the bulk space-charge region and the neutral base region became comparatively small, then the temperature was raised to the next isothermal stage. The same isothermal annealing processes were performed again at 75°C, 100°C, 125°C, 150°C, 180°C, 210°C, 240°C, 270°C. Figures 10 and 11 illustrate curves of unannealed fraction of defects in the bulk space-charge region and in the neutral base region versus time, respectively, at three different bias voltages.

Inspection of the annealing curves in Figures 8, 9, 10 and 11 reveals that there is no sudden change in annealing

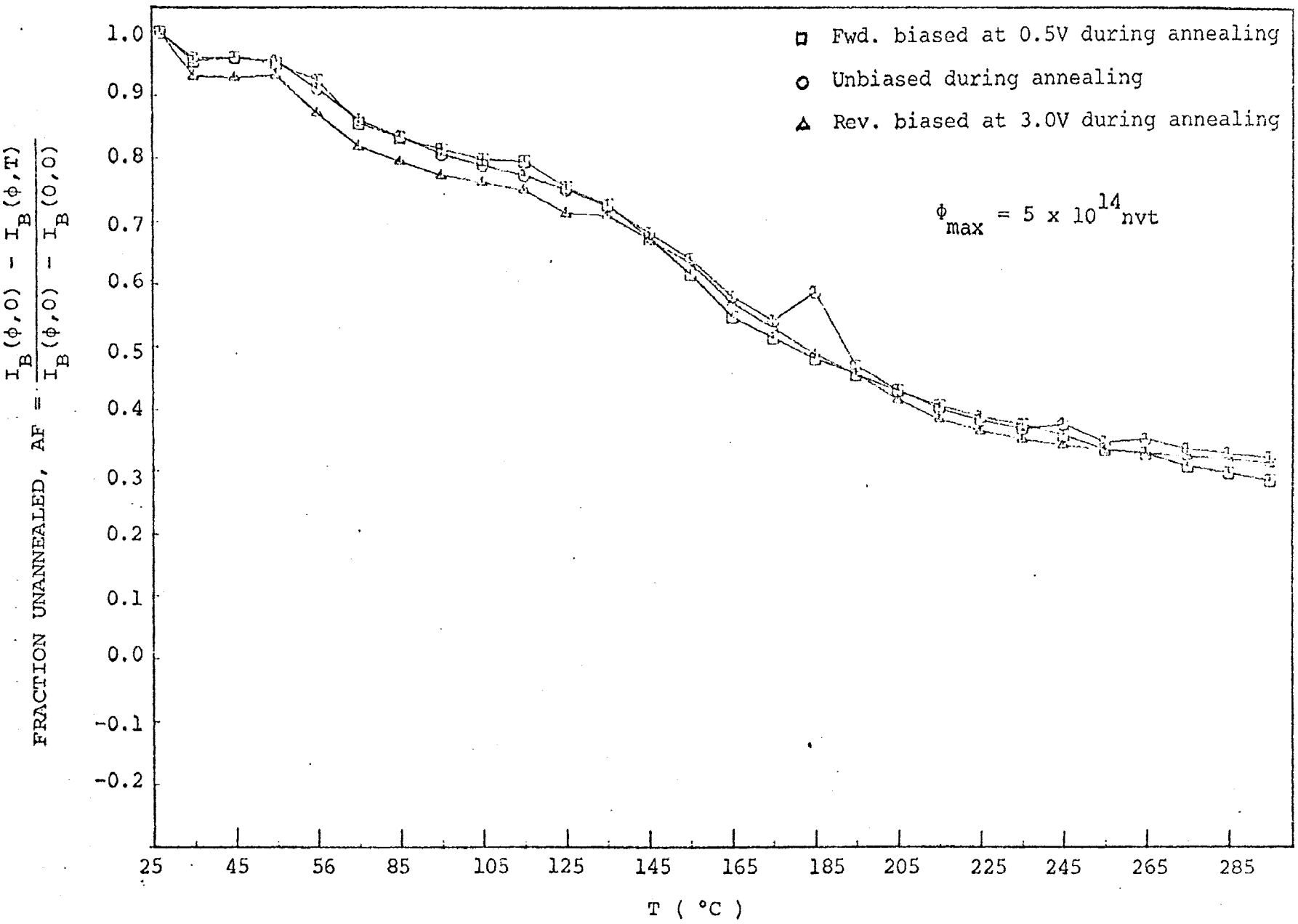


Figure 8. Isochronal annealing curves for defects in the bulk space-charge region versus temperature for devices biased at three different voltages during annealing.

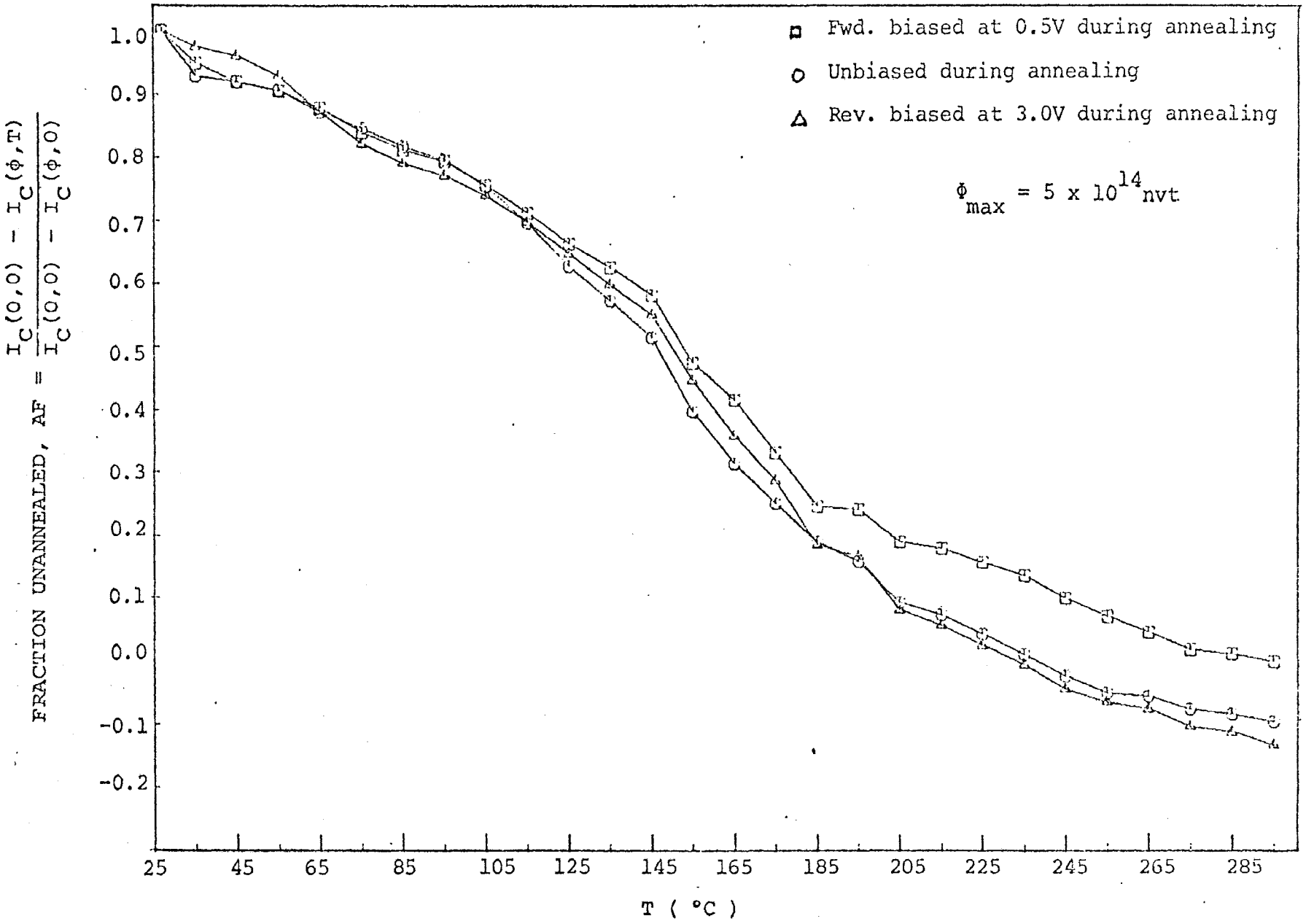


Figure 9. Isochronal annealing curves for defects in the neutral base region versus temperature for devices biased at three different voltages during annealing.

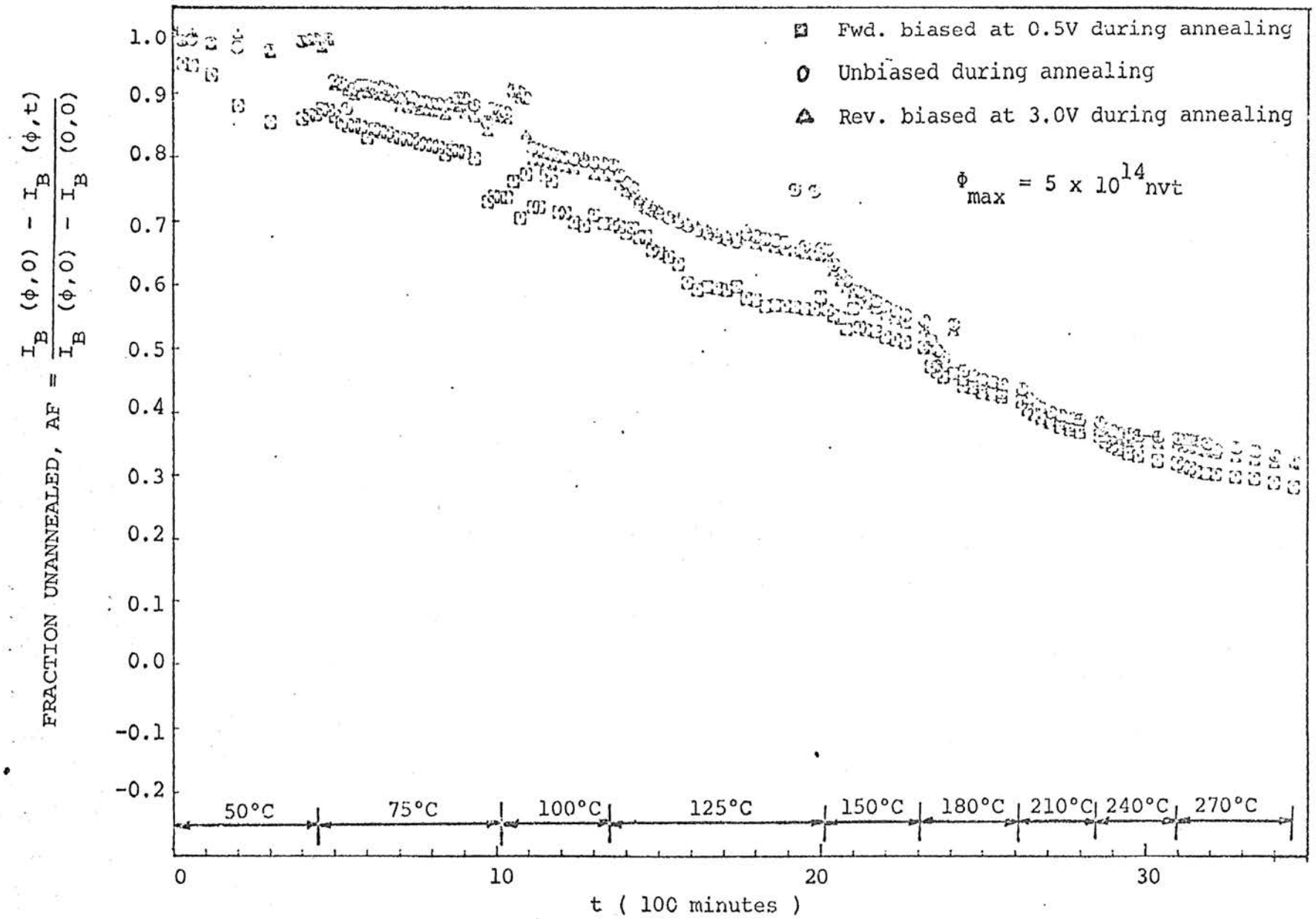


Figure 10. Isothermal annealing curves for defects in the bulk space-charge region versus time (at nine isothermal annealing temperatures) for devices biased at three different voltages during annealing.

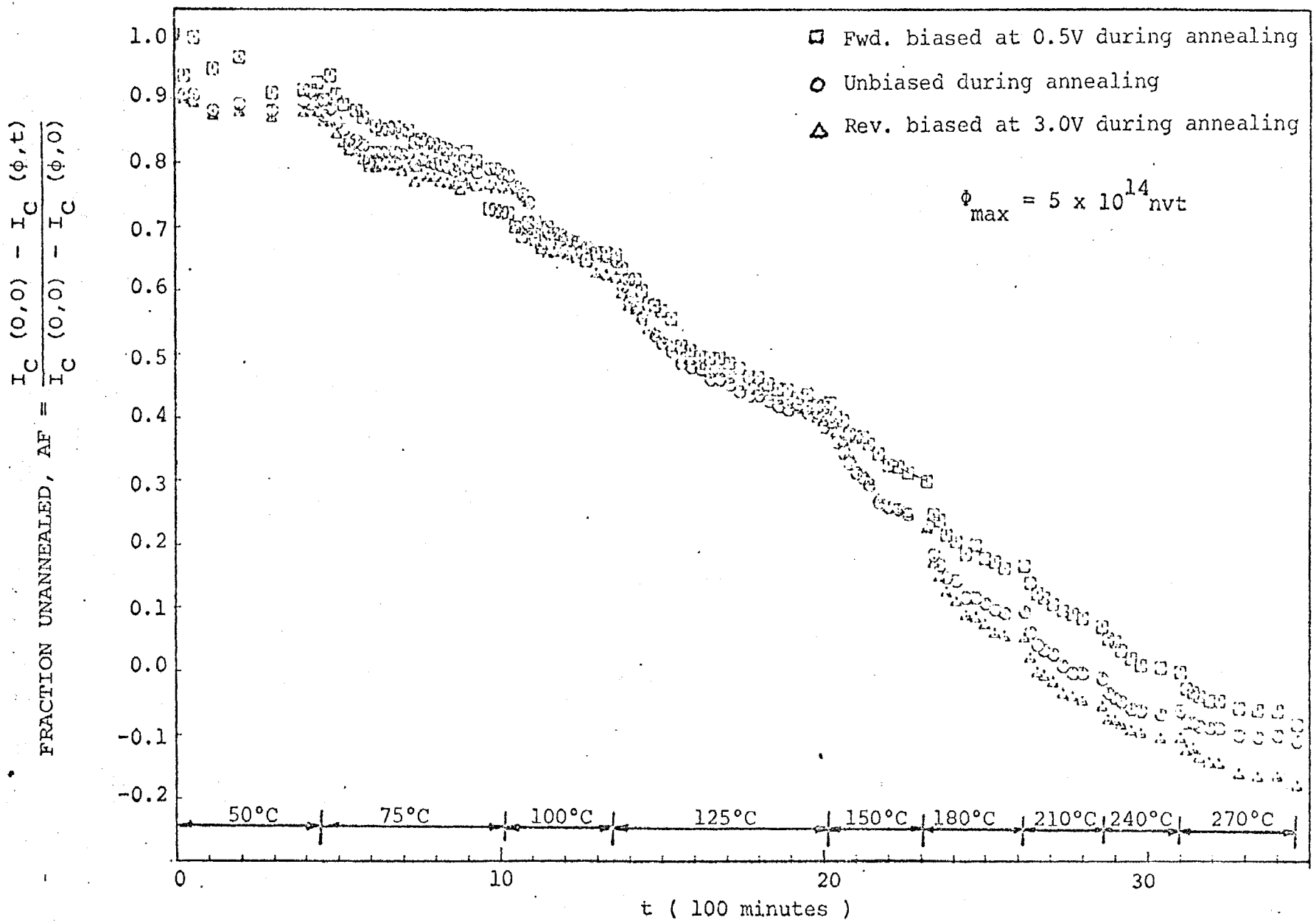


Figure 11. Isothermal annealing curves for defects in the neutral base region versus time (at nine isothermal annealing temperatures) for devices biased at three different voltages during annealing.

with respect to temperature or time. These results agree with previous work on both bulk material[13] and silicon transistors[5]. The absence of annealing steps in both the space-charge region and the neutral base region is to be expected because the type of defect introduced by neutron bombardment is normally a cluster and hence unlikely to completely anneal suddenly at any temperature or time.

The defects in the neutral base region, as represented by the changes of collector current, anneal more than 100% as shown in Figures 9 and 11. This result had been observed in other annealing experiments[5] and implies that not only annealing of neutron-induced defects took place but also annealing of other defects (e.g., oxygen vacancy complexes, interstitials etc.[5]) occurred. The improvement in the post-annealing collector characteristics (less than 20%) due to this annealing is very slight as compared to the total annealing of the collector characteristics. The devices were pre-annealed at 250°C for 12 hours in this work and this work suggests that a longer pre-irradiation baking at perhaps higher temperature would be helpful.

The unannealed fraction of defects in the bulk space-charge region increases for some of the isothermal annealing runs in the temperature range from 50°C to 100°C, as shown in Figure 10. Since reverse annealing of defects with an activation energy equal to E_c - 0.17eV in n-type silicon has been observed previously by Inuishi and his associates[14], and was attributed to an increase in the number of A-centers

(oxygen-complexes), the observed increase of the unannealed fraction of defects in the bulk space-charge region may also be caused by an increase in the number of A-centers. No increase in unannealed fraction of defects in the neutral base region was observed as can be seen from Figure 11. This may also explain why the bulk space-charge total annealing is less than the neutral base region total annealing.

Activation energies of 0.19 ± 0.04eV and 0.86 ± 0.15ev in the bulk space-charge region, 0.34 ± 0.06eV and 0.98 ± 0.18eV in the neutral base region were calculated by combining data from both isothermal and isochronal annealing of two identical devices[8]. The activation energies of 0.19 ± 0.04eV, 0.34 ± 0.06eV and 0.98 ± 0.18eV closely agree with the values found by previous investigators[14-17].

Previous analyses[17,18] have shown that negatively charged centers, which are related to defects thermally annealed in the vicinity of 200°C in n-type germanium[18,19], are annealed at a lower temperature when an electric field is impressed at the junction[17,18]. The electric field in the bulk space-charge region in the device reverse biased at 3.0V and the unbiased device is larger than that for the device forward biased at 0.5V. Therefore, the annealing rate of defects in the bulk space-charge region for the device reverse biased at 3.0V and the unbiased device should be larger than that for the device forward biased at 0.5V in the temperature range where negatively charged centers are annealed. When the device is reverse biased at 3.0V during

annealing, part of the defects originally in the neutral base region are affected by the electric field due to the extension of the junction, thus enhancing the annealing rate of defects in the neutral base region. The annealing rate of defects in the neutral base region for the device reverse biased at 3.0V should therefore be larger than that for the unbiased device and the device forward biased at 0.5V.

In the temperature range from 150°C to 180°C the annealing rate of defects in the bulk space-charge region for the device reverse biased at 3.0V and the unbiased device is larger than that for the device forward biased at 0.5V as shown in Figures 8 and 10. The annealing rate of defects in the neutral base region for the device reverse biased at 3.0V is larger than that for the device forward biased at 0.5V and the unbiased device as shown in Figures 9 and 11. The significant increase in annealing rate in the temperature range from 150°C to 180°C caused by the increase in the externally applied electric field is thought to be caused by the annealing of the negatively charged centers.

V. SUMMARY AND DISCUSSION

Operating a SA7472 silicon planar epitaxial transistor in the inverse configuration (i.e., with the emitter functioning as a collector) allows one to examine the current-voltage characteristics of an "emitter-base" junction whose volume is increased by a factor of approximately 27 times that of the normal emitter-base junction. This makes it easier to investigate the effects of neutron radiation in the space-charge region. In addition, since the carrier concentration in the emitter of such a device is about 10^5 times that of the collector, the Fermi level in the emitter region lies closer to the conduction band than does the Fermi level in the collector region. Thus, inversion layers are more easily formed in the "emitter-base" junction region when the device is operated in the inverse configuration, allowing the study of neutron-induced surface effects.

Experiments have been performed with a bias applied to the new "emitter-base" junction to change the depletion layer volume during neutron radiation. Surface effects in the form of an inversion layer adjacent to the "emitter-base" junction have been observed to cause the base current to increase by a factor of 5 to 10 in the low "emitter-base" voltage region (as shown in Figure 3), and the "emitter-base" junction capacitance to increase by a factor of approximately 2 at a fluence of 2×10^{14} nvt (as shown in Figure 2). None of the changes in minority carrier lifetime with neutron fluence are attributable to this neutron-induced

inversion layer. The "emitter-base" junction was reverse biased at 3.0V during irradiation in this experiment. This inversion layer was found to be significantly annealed at room temperature in approximately 4 weeks (as is shown in Figure 3).

Surface effects can be a very important factor in transistor circuits. Since the collector-base junction is reverse biased in the normal operating configuration, this study shows that surface effects do occur at the collector-base junction for active transistors exposed to neutron radiation. This also shows that an inversion layer is formed at the transistor surface near a junction if the surface concentration is low and if the junction is reverse biased during radiation.

A computer program using the least-squares fitting technique was used to estimate the value of the diffusion potential, V_T, by using the measured data of junction capacitance versus externally applied voltage. A decrease in the diffusion potential, V_T, was predicted on theoretical grounds and was observed experimentally following neutron radiation. The diffusion potential decreased to approximately 90 per cent of its original value at a fluence of 5×10^{14} nvt. The diffusion potential increased after isochronal annealing, but did not anneal completely to its pre-irradiation value (as shown in Figure 7).

For the annealing studies, pairs of devices with nearly identical characteristics (matched to within 10 per cent)

have been irradiated to a fluence of 5 x 10^{14}nvt, then annealed with one device of each pair used for isothermal annealing and the other device of each pair for isochronal annealing. One pair of devices was forward biased at 0.5V, the second pair of devices was reverse biased at 3.0V and the third pair of devices was unbiased for both isochronal and isothermal annealing. Activation energies of 0.19 ± 0.04eV and 0.86 ± 0.15eV in the bulk space-charge region, 0.34 ± 0.06eV and 0.98 ± 0.18eV in the neutral base region were calculated from these isochronal and isothermal annealing data. The experimental activation energies closely agree with previously calculated values[14-17]. The combination of isochronal and isothermal annealing data of two identical devices is a generally reliable method used to study the annealing of the neutron-induced defects.

The unannealed fraction of defects in the bulk space-charge region increases for some of the isothermal annealing runs in the temperature range from 50°C to 100°C. This was attributed to the increase of A-centers (oxygen-complexes)[14].

Since the annealing process of neutron-induced defects is a function of many parameters[5, 14-17] (i.e., type of defect, type of complex, electric field, injection level, temperature etc.), but certain parameters may dominate the annealing process over a particular temperature range[15], it is advantageous to study the annealing effects in small temperature ranges. This greatly simplifies the problem because fewer parameters will dominate in a small temperature range,

making it easier to study the annealing phenomenon.

The annealing rates of defects in the space-charge region and in the neutral base region were studied using the isothermal annealing curves. It was found that the annealing rates of defects both in the space-charge region and in the neutral base region were enhanced by the externally applied reverse voltage over the temperature range of 150°C to 180°C. This was also demonstrated in the isochronal annealing experiment (as seen in Figures 8 and 9). Forward bias appears to enhance the annealing of defects in the space-charge region in the isothermal annealing curves (as shown in Figure 10), whereas reverse bias appears to enhance the annealing rate in the temperature ranges from 27°C to 145°C and from 195°C to 255°C in the isochronal annealing curves (as shown in Figure 8). No solid conclusion can be drawn as to whether there is indeed a field dependence or a injection dependence by these apparent descrepencies between the isochronal and isothermal annealing curves. This should be further investigated.

At temperatures above 50°C, reverse bias enhances annealing and forward bias retards the annealing of defects in the neutral base region (as shown in Figures 9 and 11). These data indicate that the annealing rate of defects in the neutral base region is enhanced by the field, and furthermore, that the annealing rate in the p-type neutral base region is decreased by the minority carrier injection which agrees with previous work by Sander and Gregory[16].

BIBLIOGRAPHY

1. Goben, C. A., "Neutron Bombardment Reduction of Transistor Current Gain," Sandia Lab. (Publication), SCR-64-1373, 1964.

2. Goben, C. A. and Smits, F. M., "Anamolous Base Current Component in Neutron Irradiated Transistors," Sandia Lab. (Publication), SCR-64-195, 1964

3. Goben, C. A., "A Study of the Neutron-Induced Base Current Component in Silicon Transistors," IEEE Radiation Effects Conference, Ann Arbor, Michigan, 1965. IEEE Trans. on Nuclear Science, NS-12: 5, 134-146, 1965.

4. Gassner, G. E., "Variation of Inverse Parameters with Neutron Radiation in Silicon Transistors," Unpublished M.S. Research, University of Missouri-Rolla, 1968.

5. Chott, J. R. and Goben, C. A., "Annealing Characteristics of Neutron Irradiated Silicon Transistors," IEEE Trans. on Nuclear Science, NS-14: 6, 134-146, 1967.

6. Chow, M. C., "Recombination Statistics for the Neutron-Induced Base Current Component," Unpublished Ph.D. Research, University of Missouri-Rolla, 1968.

7. Hilibrand, J. and Gold, R. D., "Determination of the Impurity Distribution in Junction Diodes from Capacitance Voltage Measurements," RCA Review, 21: 245-252, 1960.

8. Meechan, C. J. and Brinkman, J. A., "Electrical Resistivity Study of Lattice Defects Introduced in Copper by 1.25-MeV Electron Irradiation at 80°K," Phys. Rev., 103: 1193-1202, 1956.

9. Easley, J. W., "The Semiconductor Device in Radiation Damage Research," 7th International Conference on the Physics of Semiconductors, Radiation Damage in Semiconductors, Academic Press, New York and London, pp. 241-363, 1964.

10. Phillips, A. B., Transistor Engineering, McGraw-Hill, New York, pp. 64; 86-91; 108-115; 270-295, 1962.

11. Messenger, G. A. and Spratt, J. P., "The Effect of Neutron Irradiation on Germanium and Silicon," Proc. IRE, 46: 1038-1044, 1958.

12. Bartling, D. L., Jenkins, C. R. and Goben, C. A., "An Automatic Data Acquisition System for Semiconductor

Device Testing," IEEE Trans. on Instrumentation and Measurement, IM-17: 1, 19-28, 1968.

13. Stein, H. J., "Introduction Rates of Electrically Active Defects in n- and p-Type Silicon by Electron and Neutron Irradiation," J. Appl. Phys., to be published, 1968.

14. Tanaka, T. and Inuishi, Y., J. Phys. Soc. Japan, 19, p. 167, 1964; Y. Inuishi and K. Matsuura, J. Phys. Soc. Japan, 18: Suppl. III, 240, 1963; as cited in reference 15.

15. Hasiggati, R. R. and Ishino, S., "Defect Mobility and Annealing in Irradiated Germanium and Silicon," 7th International Conference on the Physics of Semiconductors, Radiation Damage in Semiconductors, Academic Press, New York and London, pp. 259-273, 1964.

16. Sander, H. H. and Gregory, B. L., "Transient Annealing in Semiconductor Devices Following Pulsed Neutron Irradiation," IEEE Trans. on Nuclear Science, NS-13: 6, 53-62, 1966.

17. Davoust-Saltiel, E. and Baruch, P., "Drift Mobility of Radiation Induced Defects in Silicon," 7th International Conference on the Physics of Semiconductors, New York and London, pp. 275-280, 1964.

18. Baruch, P., "Mobility of Radiation-Induced Defects in Germanium," J. Appl. Phys., 32: 4, 653-659, 1961.

19. Waite, T. R., "Diffusion-Limited Annealing of Radiation Damage in Germanium," Phys. Rev., 107: 2, 471-478, 1957.

ACKNOWLEDGEMENTS

The author wishes to express his gratitude to his advisor, Dr. Charles A. Goben, for his efforts in guiding this Master's thesis.

Appreciation is expressed to Dr. Albert E. Bolon for his many useful suggestions and effort in reading this thesis.

A special note of thanks goes to Mr. C. R. Jenkins for his valuable assistance in the fabrication and opteration of test equipment.

The author wishes to acknowledge his co-workers for their many useful and informative suggestions and discussions.

The author is happy to acknowledge Texas Instruments for their fabrication of the special devices used in these experiments.

The author wishes to express his appreciation to the Atomic Energy Commission for their support of this research effort under contract AT(11-1)-1624.

Appreciation is expressed to Mrs. Sally J. Johnson and Mrs. Chao-Chu Chow for their help in typing this thesis.

VITA

The author was born on October 28, 1942 in Szuchuan, China. He received his primary and secondary education in Kaohsiung, Taiwan, China. He received his Bachelor of Science Degree in Electrical Engineering from the National Taiwan University in June, 1965.

The author's experience includes a position with Chinese Army Signal Corps, Taiwan, China, during the period from July 1965 to July 1966. In his capacity as Chief of a Military Radio Station, the author was responsible for the operation and design of transmitters, receivers and antennas. From December 1966 to May 1968, the author worked as a research assistant studying Nuclear radiation effects on silicon p-n junctions, at the Space Sciences Research Center, University of Missouri-Rolla.

APPENDIX A: AUTOMATIC DATA ACQUISITION SYSTEM AND DATA REDUCTION TECHNIQUES

1. General Description

The Automatic Data Acquisition System[A1] for the measurement and recording of the voltage versus current characteristics of the test devices used in most of the studies conducted is capable of current and voltage measurement with an overall absolute accuracy of ±1% of reading and a precision (repeatability) of ±0.3% of reading in the range from 10^{-10} amperes to 2×10^{-1} amperes (over 9 decades). Figure A-1 shows a block diagram of the complete Data Acquisition System plus the additional facilities necessary for obtaining the V/I Characteristics. Figure A-1 also indicates the flow paths for data and control information between the various equipments. Figure A-2 is a photograph of the system as its operation is initiated.

The heart of this system is a Control Center[A2,A3] which controls the programming, measurement and recording sequence of the system. A signal is sent to the Programmer[A2,A3] to program the John Fluke 383B Voltage-Current Calibrator which applies an emitter-base bias to the test device which is mounted in a sample holder (see Figure A-3) contained within a Delta Design MK2310 Temperature Control Chamber. The collector-base bias is supplied by a manually controlled Harrison Labs 865C Power Supply or a digitally controlled John Fluke 383B Voltage/Current Calibrator. The currents

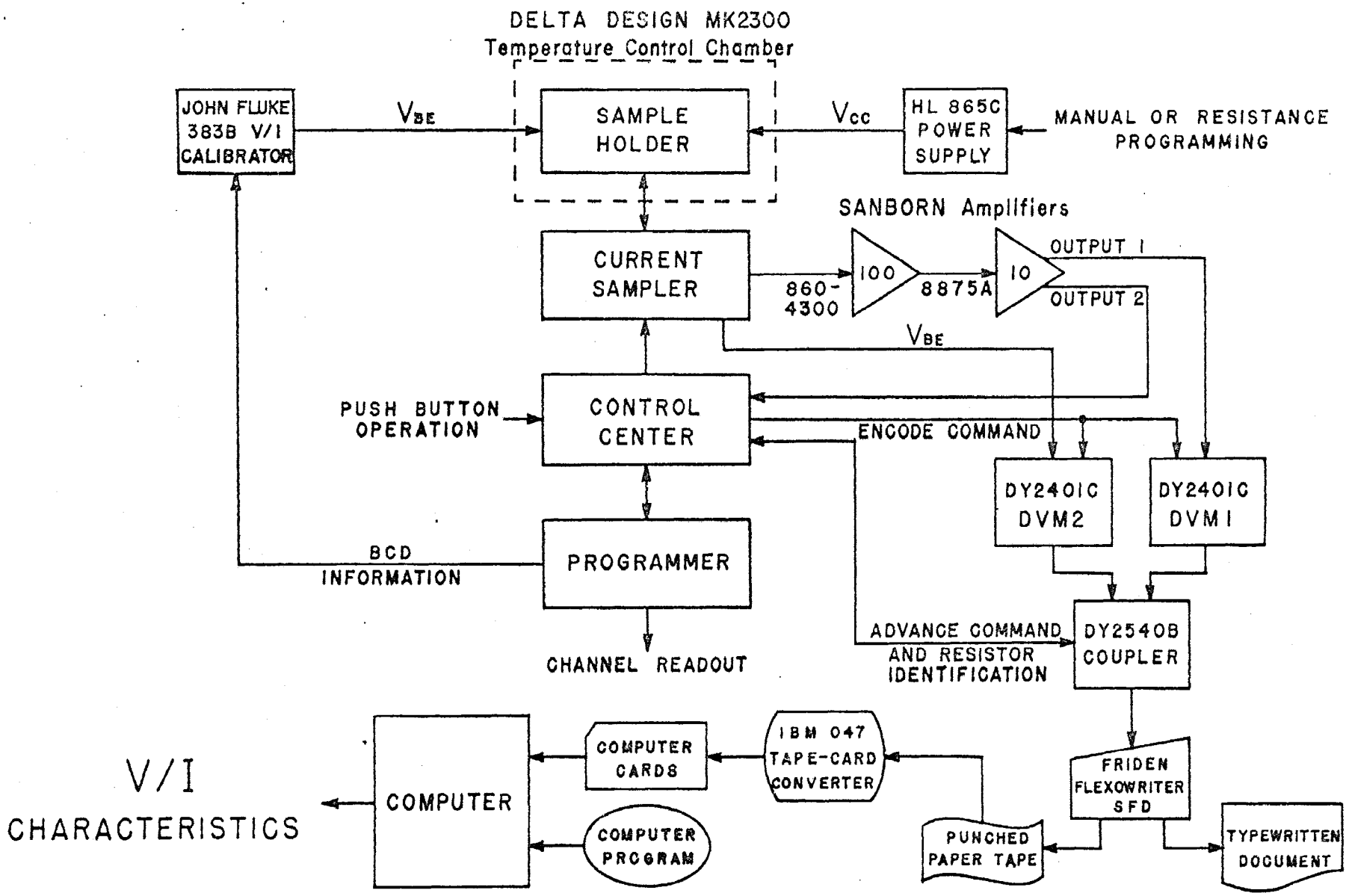


Figure A-1. Block diagram of the Automatic Data Acquisition System.

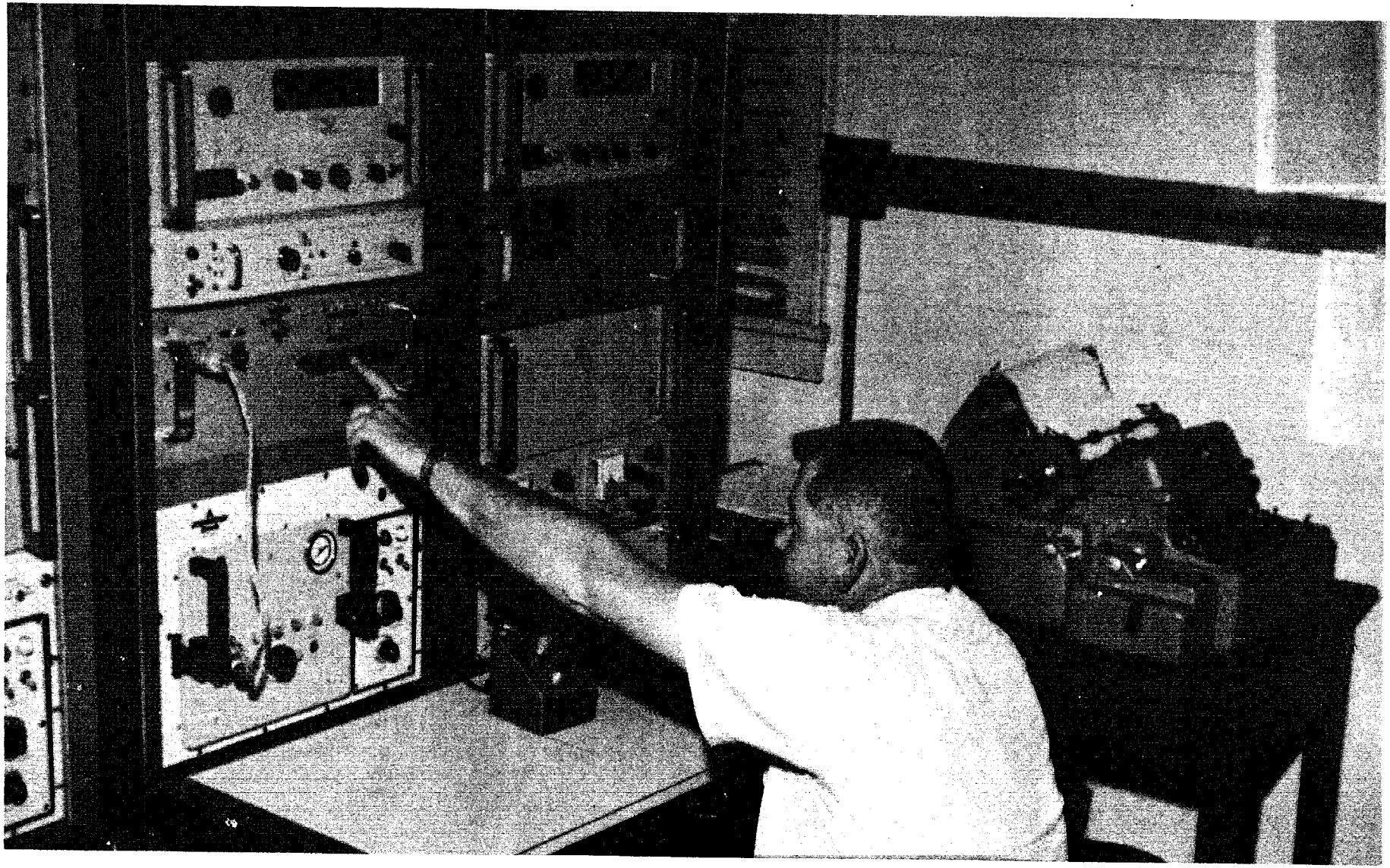


Figure A-2. Photograph of initiation of the system for a typical data run.

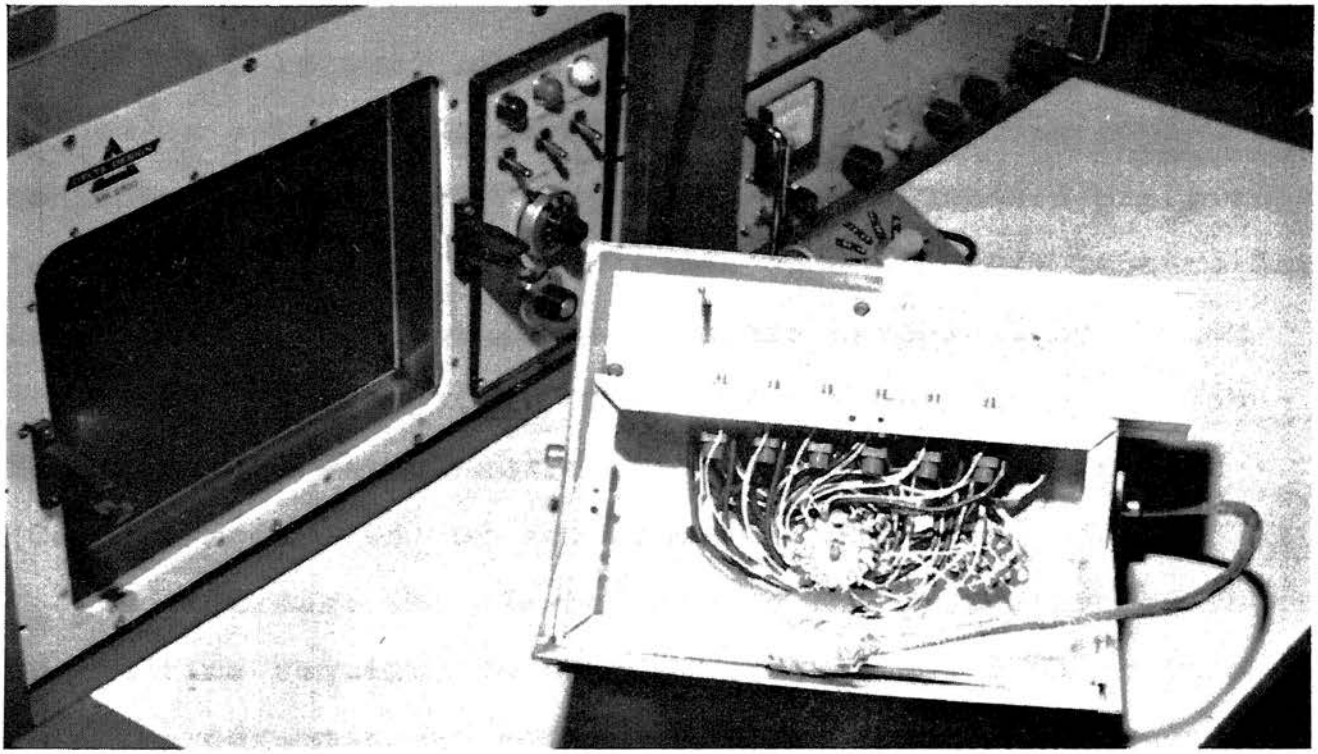


Figure A-3. Photograph of sample holder in its mounting, the heat sink standing behind the devices.

are sampled by the Current Sampler[A2,A3] whose output is amplified by a low noise Sanborn Type 860-4300 amplifier and measured by a Dymec 2401C-M31 Digital Voltmeter. The emitter-base bias voltage is measured by a second Dymec 2401C-M31 Digital Voltmeter. The voltmeter readings are recorded along with resistor identification information in digital form supplied by the Autoranging Current Sampler[A2,A3]. This information is serialized by a Dymec 2540B Coupler and recorded on a Friden Model SFD Flexowriter in both type-written form and on punched paper tape. The punched paper tape is converted to IBM punched cards on an IBM 047 Tape-to-Card Converter, and the punched cards are processed by an IBM 360-50 Digital Computer. The computer output is the tabulated voltage versus current characteristics and a plot (Calcomp Model 566) of the tabulated values.

To increase the flexibility of the system and to shorten the time required to change programming, a paper tape reader-programmer was added. Since a paper tape reader-programmer capable of performing the desired functions was not available commercially, one has been designed and fabricated. The addition of this paper tape reader-programmer permits the programming of either or both John Fluke 383B Voltage/Current Calibrators while greatly reducing the time required to change from one set of pre-programmed values to another.

A program was written for the processing of the output data from the Automatic Data Acquisition System by the IBM 360-50 Computer. This program performs four major

functions.

First, computation of device voltages and currents from the input voltage and resistance data with corrections made for the voltage drop across the current sampling element.

Second, interpolation is made to values of emitter-base voltage which are integral multiples of 10.0 millivolts. This interpolation provides a means of comparing currents and current gains at fixed values of base-emitter voltage.

Third, the applied base-emitter voltage versus base and collector currents and current gain is provided in tabular form together with heading information which includes device identification and measurement conditions.

Fourth, a machine plot (Calcomp Model 566) of input voltage versus logarithm of base current and logarithm of collector current, with printed device identification and neutron fluence, is output for use by the investigator in comparison studies. Each plotted page is a 14 x 10 inch graph of the form log(I) versus V_{BE}. This program will return a plot of the logarithms of I_B and I_C versus V_{BE} for each device while a second plot program returns one plotted page depicting either $\log(I_C)$ or $\log(I_B)$ versus V_{BE} curves for as many devices as desired.

The run time for the first plot program is approximately 2½ minutes per device and the run time for the second plot program is approximately one minute per device.

The test device is located in the Sample Holder, as shown at the top of Figure A-1 which is, in turn, inside the

Delta Design MK2300 Temperature Control Chamber. The MK2300 is a precision environmental temperature test chamber capable of maintaining any temperature from -100°F (-73.4°C) to 600°F (+315.6°C) within ±0.1°C. The forced air circulation system is closed and powered by a 140 CFM blower. The chamber is heated by applying full wave power to a pair of bobbin wound nichrome 720 watt heating elements controlled by the "heat" solid state switch and is cooled by injecting liquid CO_2 into the air stream through an expansion nozzle controlled by the "cool" solid state switch.

Comparing the resistance of a temperature probe to the resistance of a "Temperature Set" potentiometer, the controller senses when to apply heat, coolent, or withold both so as to obtain and maintain a selected temperature in the chamber.

2. Cyclic Operation

The data for the base current versus voltage characteristic and collector current versus voltage characteristic is obtained with the device in, respectively, the Base Current Measurement Circuit shown schematically in Figure A-4, and the Collector Current Measurement Circuit shown schematically in Figure A-5. The Sampling Resistance appears in the measurement circuit as a physical resistance having one of nine discrete values, ranging from 17 milliohms to one megohm, each approximately a decade apart from the next. The Sampling Resistance is determined by the parallel combination

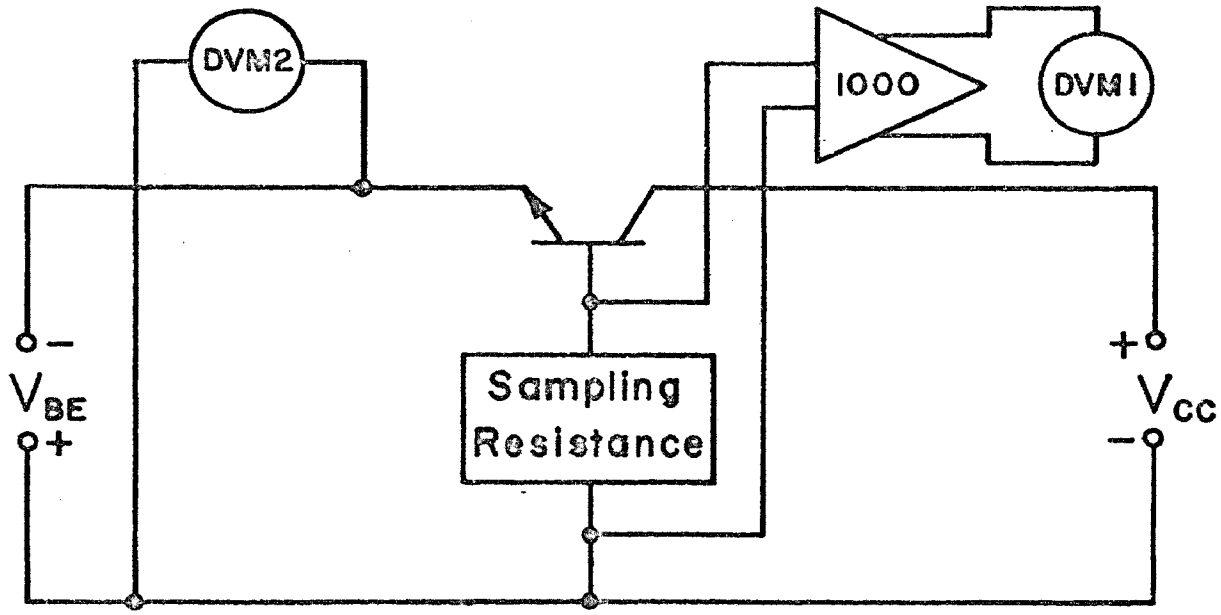


Figure A-4. Base current measurement circuit.

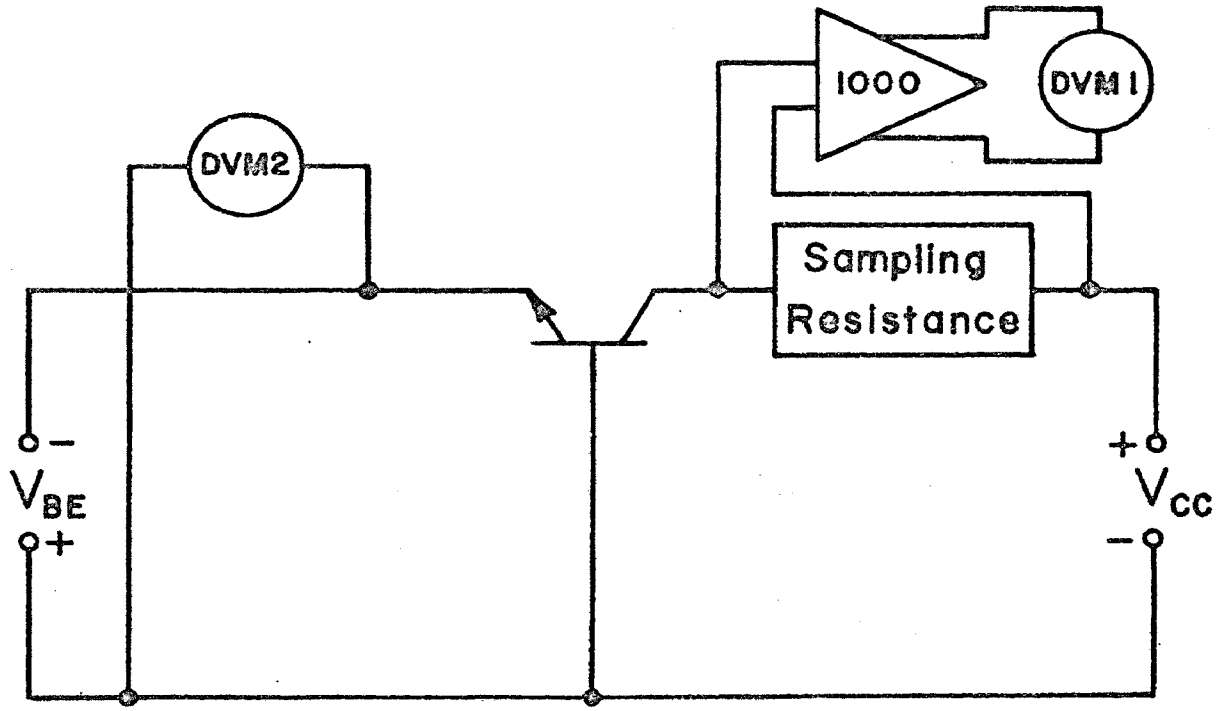


Figure A-5. Collector current measurement circuit.

of all resistors which are in the measurement circuit after the autoranging procedure is performed. The value of the Sampling Resistance as shown in Figure A-6 is, therefore, 17 milliohms.

The system is designed to perform a particular sequence of events in obtaining test data from a semiconductor device. In simplified terms, the sequence of events for one typical cycle of the system is as follows:

1. With the test device initially in the Base Current Measurement Circuit (Figure A-4) and with a particular value of base-emitter bias and collector supply voltage applied to the device, the system autoranges selecting one of the nine possible values of the Sampling Resistance such that the voltage drop across the Sampling Resistance is normally greater than 0.5 millivolts and less than 5 millivolts. This autoranging procedure has been explained in detail in reference A2.
2. The digital voltmeters encode and their readings are recorded.
3. The device is switched into the Collector Current Measurement Circuit (Figure A-5).
4. The two digital voltmeters again encode and their readings are recorded
5. The device is switched back into the Base Current Measurement Circuit (Figure A-4).
6. A new value of base-emitter bias, V_{BE}, is applied

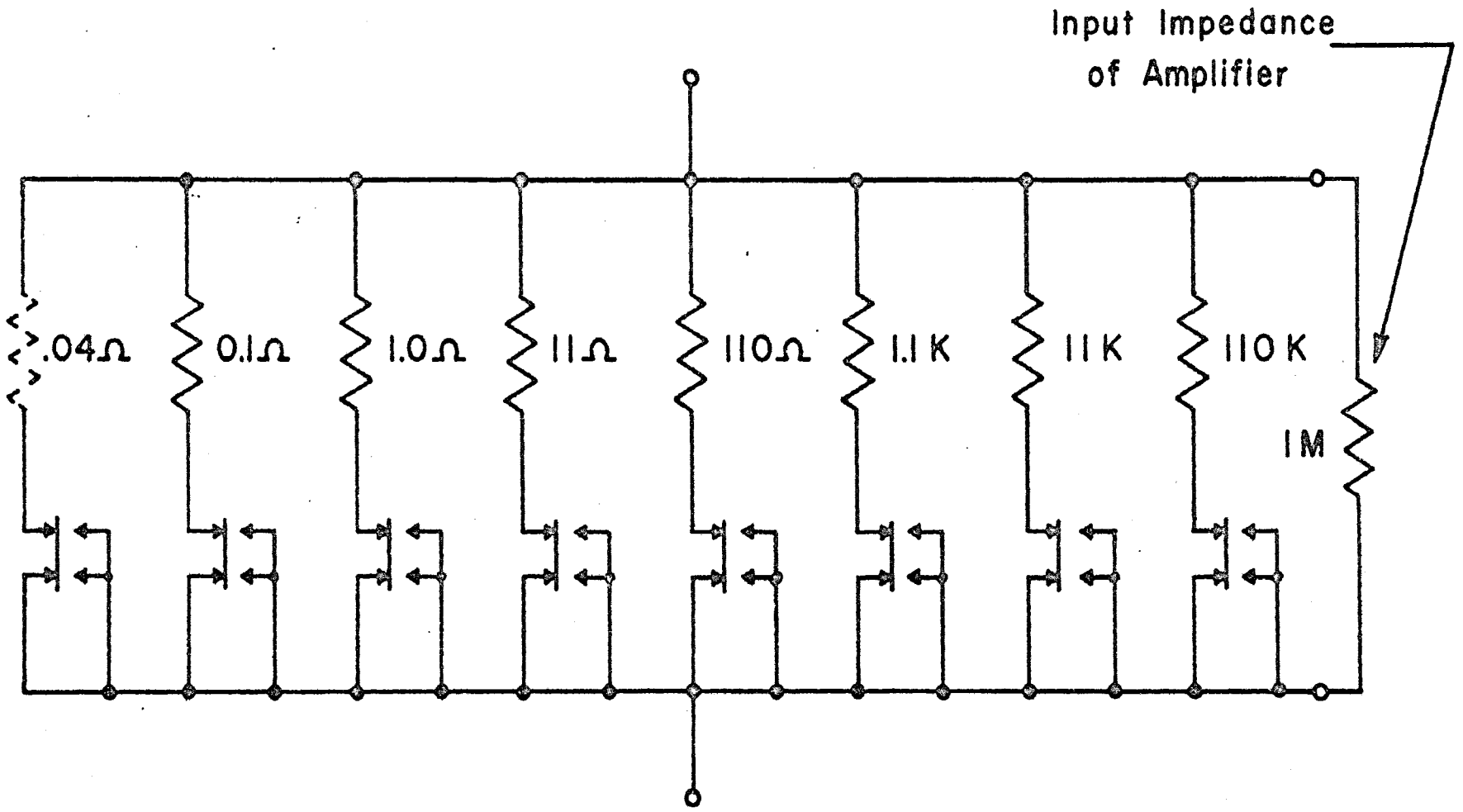


Figure A-6. Sampling resistance.

to the device and the sequence is repeated.

These steps define one cycle of the system. The system continues cycling in this manner until all of the required pre-programmed values of V_{BE} (59 values of V_{BE} are available if needed) have been used.

The collector supply voltage, V_{CC}, can be set manually before a test run in which case it remains constant during that test run, or a series of voltages can be programmed for a test run. In this second case, the emitter supply voltage, V_{BE}, is usually held constant.

An additional method of operation allows one to measure base current only or collector current only. This method of operation is selected by the MODE switch on the front panel of the control center.

REFERENCES

A1. Goben, C. A., "Nuclear Radiation Effects on Silicon p-n Junctions," Technical Progress Report, Document COO-1624-11, Space Sciences Research Center, University of Missouri-Rolla, 1968.

A2. Bartling, D. L., "An Automctic Data Acquisition System for Semiconductor Device Testing," M.S. Thesis, Library, University of Missouri-Rolla, 1967.

A3. Bartling, D. L., Jenkins, C. R. and Goben, C. A., "An Automatic Data Acquisition System for Semiconductor Device Testing," IEEE Trans. on Instrumentation and Measurement, IM-17: 1, 19-28, 1968.

APPENDIX B: CAPACITANCE-VOLTAGE MEASURING SYSTEMS

Two systems were used for the measurement and recording of capacitance versus voltage data[B1]. The alternative capacitance measuring systems use a Micro-Instruments Model 1201DS Digital Capacitance Tester as the basic measuring instrument. A Dymec 2901A Master Scanner/Programmer and a Dymec 2902A Slave Scanner/Programmer are used for control and programming. The Dymec 2901A Master Scanner/Programmer and the Dymec 2902A Slave Scanner/Programmer are electronically controlled stepping switches which provide automatic scanning of 25 signal inputs each. The test devices in the alternative systems are mounted in a Delta Design MK2310 Temperature Control Chamber (see Appendix A).

The digital Capacitance Tester is a direct reading high speed instrument for accurate capacitance measurements. A guarded two terminal test jig is permanently attached to the front panel of the instrument. This test jig is guarded with a signal similar to the test signal to neutralize the capacitance effects of the component leads; thus the instrument measures direct capacitance rather than grounded capacitance. Three BNC coaxial connectors for remote or special test jigs are provided on the front panel. The connectors provide for a test signal, a guard signal and a return for use with remote or special jigs. The Coarse Zero Control may be used to neutralize up to 100 pF of capacitance added by the cable and jig.

A digital output connector is provided on the Digital Capacitance Tester. This connector provides a print command signal as well as digital information to operate the Hewlett-Packard R66-562AR Digital Recorder. The recorder is controlled by means of a "Print" switch located on the front panel of the instrument. The output is BCD 1248 logic.

In the first alternative capacitance measuring system, a start command advances the scanner/programmer which digitally programs a voltage or current on a John Fluke 383B Voltage/Current Calibrator. This voltage or current is applied to the device under test. A capacitance reading is taken by a Micro Instrument Digital Capacitance Tester 1201DS and recorded on a Hewlett-Packard R66-562AR Digital Recorder together with the applied voltage which is measured by a Dymec 2401C-M31 Digital Voltmeter. The printed record is punched on IBM cards and processed by the IBM 360-50 Digital Computer. The block diagram for the system is shown in Figure B-1.

Alternatively, when the Automatic Data Acquisition System described in Appendix A is not in use for voltage-current measurements, the Dymec 2401C-M31 Digital Voltmeters, Dymec 2540B Coupler and Friden SFD Flexowriter may be used as the output medium. For this mode of operation the frequency output (proportional to capacitance) of the Micro-Instruments 1201DS Capacitance Bridge is measured by one of the DVM's in the Automatic Data Acquisition System while the other DVM measures the potential applied to the device under

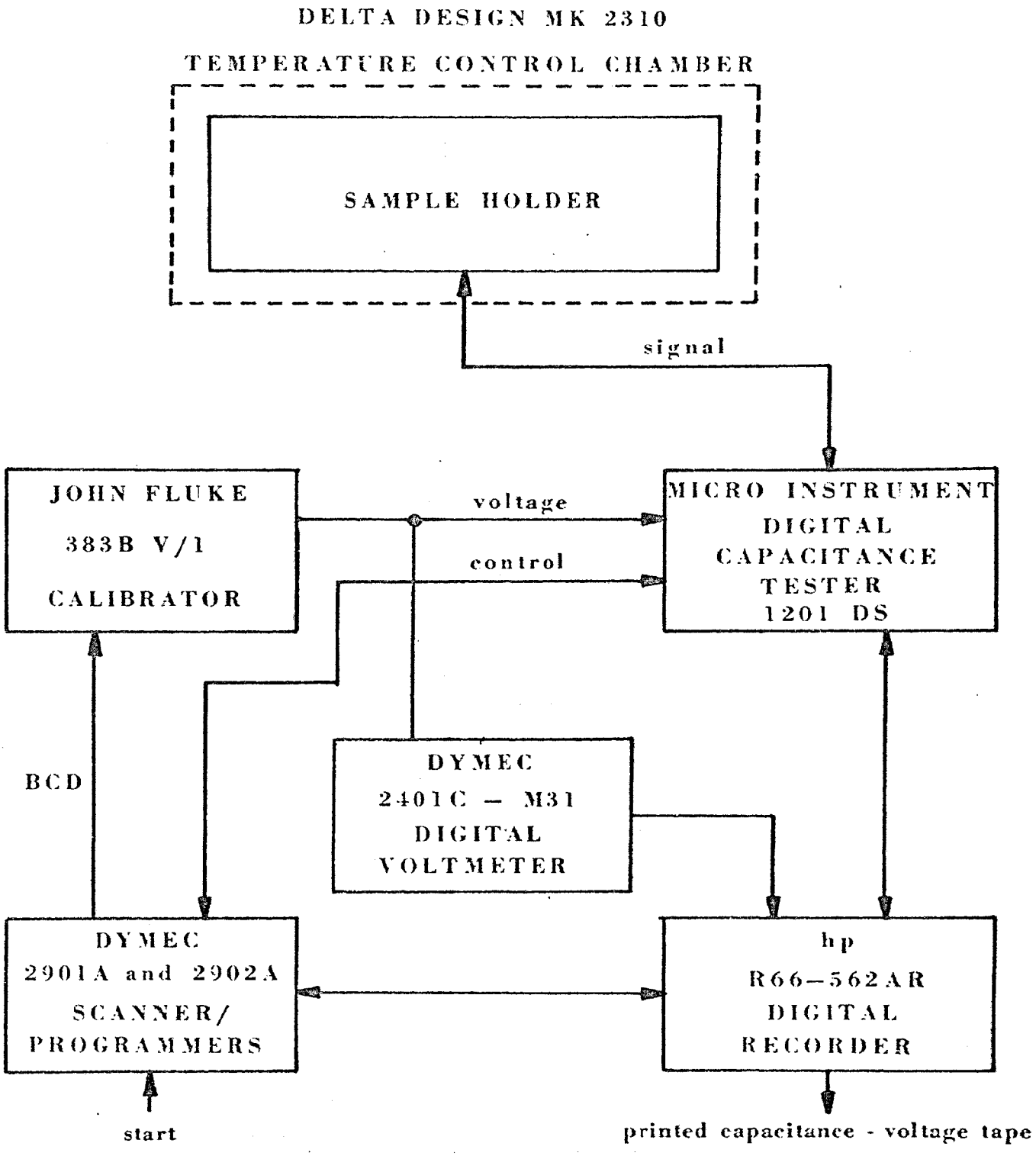


Figure B-1. Capacitance-voltage measurement system.

test. This information is then serialized by the Dymec 2540B Coupler and then printed as output by the Friden SFD Flexowriter on both punched paper tape and typewritten copy. Data processing is accomplished in a similar manner to that described for the Automatic Data Acquisition System. The block diagram of the alternative system for the capacitance-voltage measurements is shown in Figure B-2.

To facilitate the inter-connection of the Automatic Data Acquisition System and the Capacitance-Voltage System for this alternative mode of operation, a single cable was constructed carrying all data, control and signal lines. When the two systems are used separately, shorting plugs are placed over the chassis connectors on the two systems.

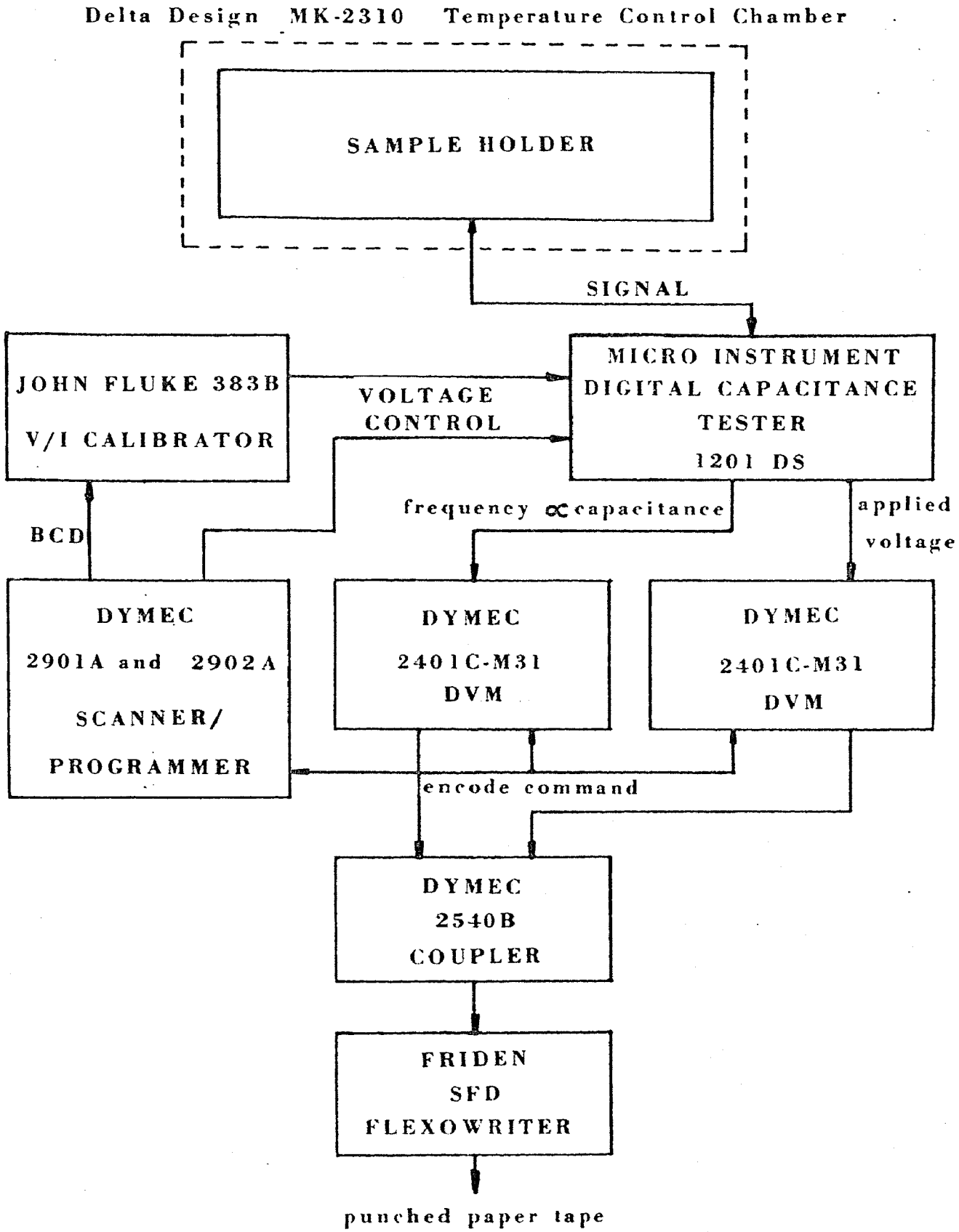


Figure B-2. Capacitance-voltage system block diagram.

REFERENCE

B1. Goben, C. A., "Nuclear Radiation Effects on Silicon p-n Junctions," Technical Progress Report, Document COO-1624-11, Space Sciences Research Center, University of Missouri-Rolla, 1968.

APPENDIX C: MINORITY CARRIER LIFETIME MEASUREMENT

1. Reverse Recovery Characteristics of Diodes

When a diode is switched from conduction in a forward bias to a reverse bias condition, instead of a high impedance immediately appearing across the diode, a momentary low impedance, which is indicated by a very low voltage across the diode, immediately occurs after the switching. This is due to the storage of minority carriers in the semiconductor material.

As the junction is suddenly reverse biased the excess minority carriers must either be swept out of the junction or recombine with excess majority carriers before a high reverse impedance can be obtained.

A typical display of diode reverse recovery characteristics is shown in Figure C-1. In Figure C-1, there are

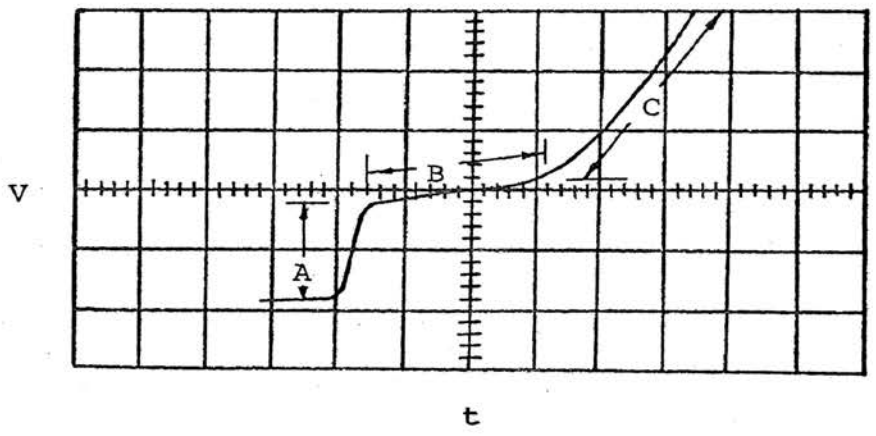


Figure C-1. Typical display of diode reverse recovery characteristics.

three areas of particular interest. These areas are desig-

nated by A, B and C. The sudden voltage drop at area A occurs at the time when forward conduction ceases. During forward conduction, this voltage drop is produced by the internal series resistance across the diode[C1]. When forward current is cut off, this voltage drop disappears, producing the voltage step. Immediately after the sudden drop at area A the voltage decays exponentially for a relatively long period of time (area B). During this interval, minority carriers in the semiconductor material are being swept out by the reverse current. The length of time required for the reverse current to remove the minority carriers gives an indication of the amount of charge stored in the material. The stored charge is found to be proportional to the forward current passing through the junction just before the diode is switched off. If zero reverse current is drawn from the diode, the voltage decay is due entirely to the recombination of minority carriers. By measuring the rate at which the voltage across the diode decays for this case, the effective lifetime can be found.

When the minority carriers in the semiconductor material have either been swept out or have recombined, the depletion region increases at the junction due to the movement of the majority carriers away from the junction. Further reverse current is then required to charge the capacitance of this depletion region (area C). This accounts for the rise in voltage across the junction. The junction capacitance is also dependent on the voltage. The capacitance does not re-

main constant, but varies with the voltage across the junction.

2. The Effective Lifetime of Minority Carriers

During the period of forward current conduction, excess minority carriers are injected into the semiconductor material. These excess minority carriers are in addition to the normal number of minority carriers present at room temperature due to the formation of electron-hole pairs. The effective lifetime of these excess minority carriers is the time required for the number of the minority carriers to decrease to 36.7% (1/e) of the original number after termination of the forward current. The effective lifetime expresses the relative rate at which the minority carriers recombine and is a constant for a given diode at a particular absolute temperature. It does not depend on either the forward or the reverse current drawn from the diode. Effective lifetimes should be specified with the temperature at which the measurements were made.

When the measured time (t) is small compared to the effective lifetimes τ and where kT/q is much smaller than the voltage across the diode, the approximation for the effective lifetime shown below holds[C1]:

$$\tau \simeq \frac{kT}{q} \cdot \frac{\Delta t}{\Delta V} \qquad \text{(C-1)}$$

At room temperature, equation (C-1) becomes

$$\tau \ (300°K) \simeq \frac{0.026}{(\Delta V/\Delta t)} \qquad (C-2)$$

In equation (C-1), it is assumed that t is small compared to τ. This means that the decay rate of the voltage across the junction should be measured just after the forward current is switched off. Mathematically stated, $\Delta V/\Delta t$ should be measured as $t \to t_o$, where t_o is the time when the forward current is switched off. The assumption that kT/q is much smaller than the voltage across the diode also holds quite generally as $t \to t_o$. Therefore, equation (C-2) should be rewritten as:

$$\tau \ (300°K) \simeq \frac{0.026}{(\Delta V/\Delta t)}_{t \to t_o} \qquad (C-3)$$

Figure C-2 shows a typical waveform used to measure the effective lifetime of minority carriers. The Tektronix Oscilloscope Type 555[C2] with the Tektronix Type S Recovery-time plug-in Unit[C3] is used for the measurements.

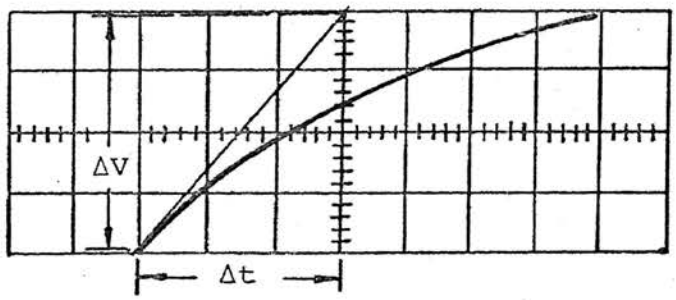


Figure C-2. Tangent line for calculating the voltage decay rate across the diode.

The waveforms used to measure the effective minority carrier lifetime were photographed by a Tektronix Type 100 camera with a Polaroid back. The pictures for each device at both emitter-base and collector-base junctions have been taken at every irradiation step. Figure C-3 shows two typical pictures which are used to illustrate the decrease in minority carrier lifetimes.

3. Minority Carrier Lifetimes in the Base and Collector Regions of a Junction Transistor

For measuring the lifetimes of a transistor, both the emitter-base and collector-base junctions can be treated as diodes. Using the method described above, the values of τ_{BE} and τ_{BC} for the emitter-base and collector-base junctions, respectively can be calculated. The minority carrier lifetimes in the base and collector regions are τ_B and τ_C, respectively, and are related to τ_{BE} and τ_{BC} according to:

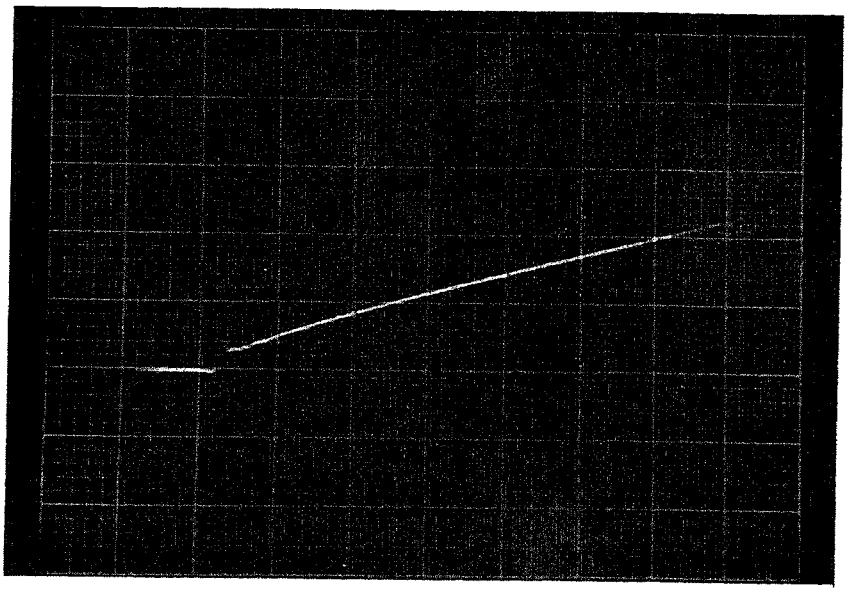
$$1/\tau_B + 1/\tau_C = 1/\tau_{BC}, \tag{C-4}$$

and,
$$1/\tau_B \simeq 1/\tau_{BE}, \tag{C-5}$$

or,
$$\tau_B \simeq \tau_{BE}, \tag{C-6}$$

$$\tau_C \simeq (\tau_{BE} - \tau_{BC})/\tau_{BC} \cdot \tau_{BE}. \tag{C-7}$$

Equations (C-6) and (C-7) were used to calculate the minority carrier lifetimes of a transistor throughout this investigation.

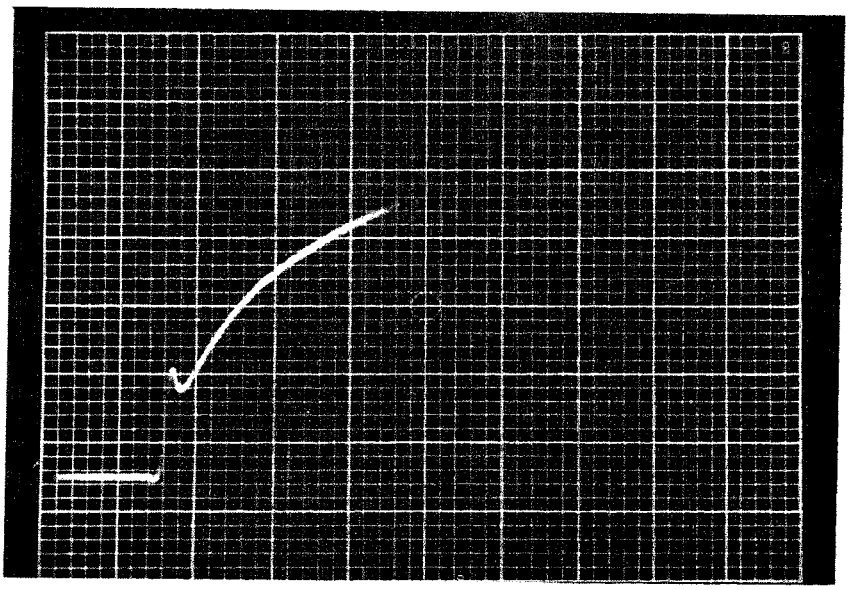


$\Phi = 0$

$$\tau \simeq \frac{0.026}{\frac{(0.05).(0.6)}{(0.1).(1.6)}}$$

$\simeq$ 139.2 ns

(at 300°K)



$\Phi = 6 \times 10^{13}$ nvt

$$\tau \simeq \frac{0.026}{\frac{(0.05).(0.4)}{(0.1).(0.2)}}$$

$\simeq$ 26 ns

(at 300°K)

Figure C-3. Photographs from which measurements of τ_{BE} at two different fluences are made.

REFERENCES

C1. Lederhandler, S. K. and Giacoletto, L. J., "Measurement of Minority Carrier Lifetime and Surface Effects in Junction Devices," Proc. IRE, 43: 477-483, 1955.

C2. "Tektronix Type 555 Oscilloscope Manual," Tektronix Inc., Beaverton, Oregon, 1964.

C3. "Tektronix Type S Plug-in Unit Manual," Tektronix Inc., Beaverton, Oregon, 1960.

APPENDIX D: NUCLEAR REACTOR FACILITY AND IRRADIATION PROBLEMS

1. Nuclear Reactor Facility

The neutron irradiations used in this investigation were performed at the Research Reactor of the University of Missouri-Rolla. This reactor is used both for laboratory training and research by the faculty and students of the University of Missouri-Rolla and other nearby universities. A table of the major reactor characteristics of the Research Reactor of the University of Missouri-Rolla is illustrated in Figure D-1.

The Research Reactor of the University of Missouri-Rolla is a "swimming pool" type reactor, installed in a windowless, concrete, brick and steel structure. The pool consists of a thick walled pit, 19 feet long, 9 feet wide and 27 feet deep, containing 32,000 gallons of pure water. The reactor core is suspended near the bottom of the pool and is covered with some 19 feet of shielding water. The water is continuously purified by an ion exchanger, which removes cations and anions, preventing corrosion and contamination.

The reactor grid plate, containing several rows of holes and 22 fuel elements, is a racklike aluminum tray. Open positions in the grid plate are available as sample holders in experiments. Position B2, (see Figure D-2). which is mapped for fast flux irradiations, was used in this experiment. The maximum fast flux (E > 0.01MeV) available

Type	Swimming pool type (modified BSR-type), housed in a windowless, concrete, brick and steel structure.
Core	Heterogeneous 90% U-235 enriched uranium oxide-Aluminum-water.
Moderator	Light water.
Reflector	Light water.
Coolant	Light water.
Biological shield	Light water and normal concrete.
Critical mass	Approximately 2.7 kilograms of U-235.
Power level	Up to 200 kw.
Maximum thermal flux	1.5×10^{12} neutrons/cm^2-sec.
Maximum fast flux (E > 10 keV)	2.25×10^{11} neutrons/cm^2-sec.
Fuel elements	MTR type; each fuel element has 10 fuel plates, each plate approximately 17 gms of U-235. Each fuel element is 3"x 3"x 36". The reactor has 22 full fuel elements: 1 left hand half elements, 2 right hand half elements, and 4 control rod elements (3 shim-safety rod, 1 regulating rod).
Auxiliary equipment	Neutron diffraction multi-channel analyzer, nuclear counting equipment; neutron generator, subcritical assembly, neutron chopper.

Figure D-1. Table of technical data for the UMR Research Reactor.

A1	A2	A3	A4	A5	A6	A7	A8	A9
B1	B2	B3	B4	S	B6	B7	B8	B9
C1	C2	C3	F	F	X	O	C8	C9
D1	D2	F	X	F	F	F	F	D9
E1	E2	F	X	F	X	F	F	E9
F1	F2	PT	F	F	F	PT	F8	F9

F = Fuel
S = Source
O = Sample Rotator
X = Control Rods
PT = Pneumatic Transfer Tubes

Figure D-2. Core configuration 31-T.

at 200 kW for position B2 is 2.25×10^{11} neutrons/cm^2-sec.

Nickel foils were used to determine the fluence levels for each irradiation. Dosimetric measurements for the neutron irradiations were performed at the reactor.

A photograph of the sample holder which was used for the transistors in all the irradiations is shown in Figure D-3.

2. Irradiation Problems

The transistors used in this neutron radiation effects study were irradiated in a double-walled aluminum sample holder having the inner space filled with boron carbide. The boron carbide shield is needed to allow only fast neutrons (E > 10keV) to bombard the devices. Boron carbide has a high capture cross-section for slow (E < 10keV) neutrons.

The aluminum used in the fabrication of the sample holder contained impurities whose radioactive half-life was long compared with aluminum. As a result, the sample holder could not be removed from the pool until this radioactive decay decreased to a point which was considered safe. A cadmium cylinder was used to shield the sample holder from the thermal neutrons causing this activation. This allowed the samples to be removed from the pool on the day that they were irradiated.

At higher fluence levels, the temperature inside the sample chamber would tend to increase, requiring a flow of nitrogen through the sample chamber during irradiation to

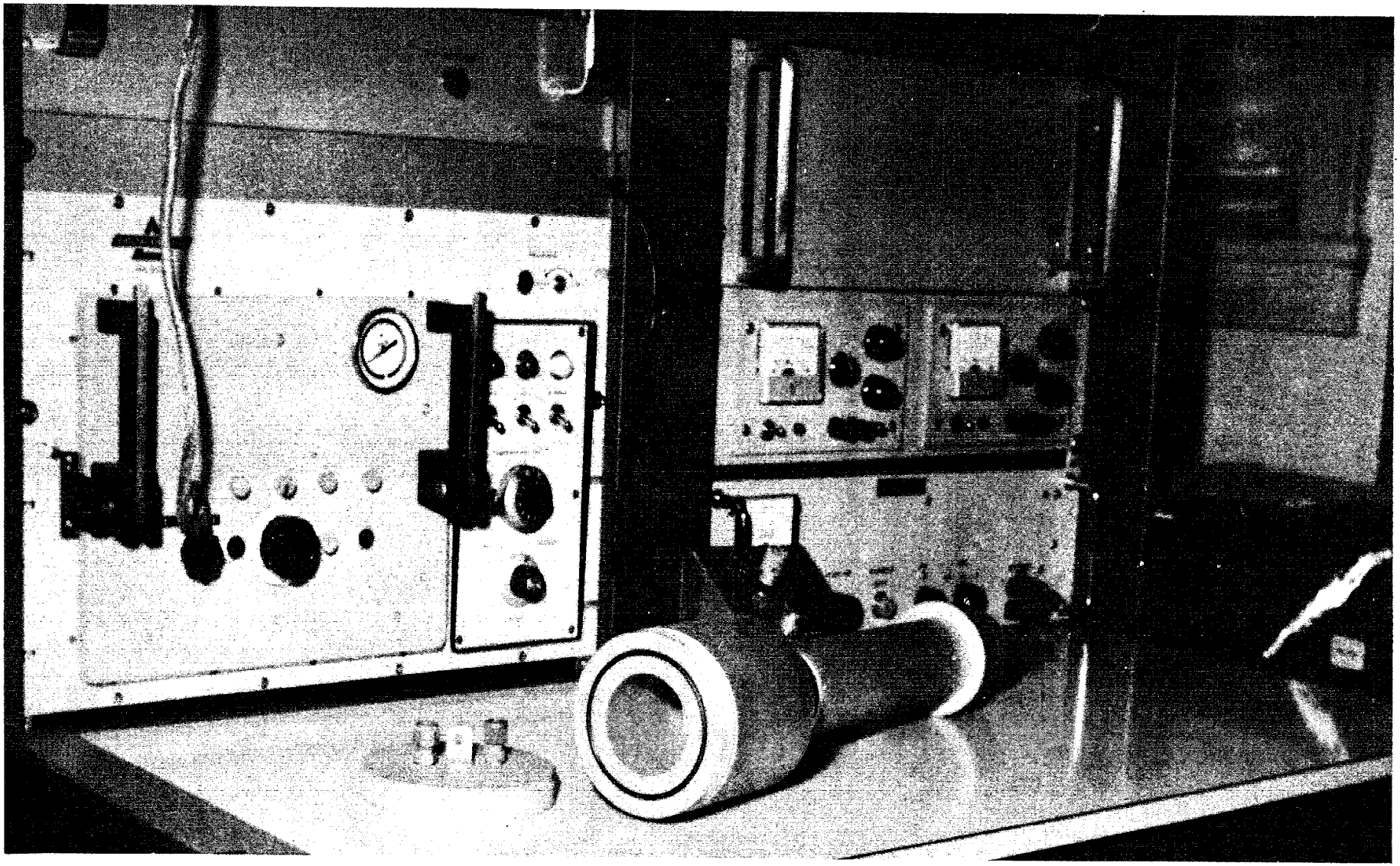


Figure D-3. Photograph of sample holder.

cool the devices. This coolant was necessary to insure that annealing did not take place during irradiation.

Further complications were presented by the reactor being operated at 200kW in other experiments which raised the water temperature at times to as high as 57°C. This required the use of nitrogen coolent as long as the devices were in the reactor pool, otherwise, annealing would have taken place.

APPENDIX E: HISTORY OF THE RESEARCH IN THIS AREA

The observed decrease in transistor current gain resulting from exposure of transistors to neutron irradiation[E1] had, in the past, been attributed primarily to the neutron-induced reduction in minority carrier lifetime in the base region, that is, to the resultant reduction of the base recombination term[E2-E6]. Recent investigations[E7,E8] have shown that the fall off of the transistor current gain at low currents in non-irradiated transistors is caused by a reduction in the emitter efficiency. This suggested that emitter efficiency was important in transistor gain changes resulting from irradiation. To ascertain the role of emitter effeciency, a more detailed study of the degradation of transistors in a radiation environment was required. Such a study was reported by Goben and Smits[E9] in 1964.

Several components of base current have been identified in non-irradiated transistors. The first of these, the bulk recombination-generation current, or the ideal diffusion current for uniform base transistors was first suggested by Shockley[E10] and later extended to the non-uniform base situation by Moll and Ross[E11]. It has a voltage dependence of exp(qV/kT). The second component is a recombination current in the transition (space-charge) region. The voltage dependence of this second component approximates exp(qV/2kT) at low current densities[E12]. A third component, the surface-perimeter component, has been found to originate at the

perimeter of the emitter[E7,E8,E13], that is, where the emitter-base junction intersects the surface. Iwersen et al.[E7] suppressed this component by placing a guard ring on the emitter and applying a bias from emitter contact to guard ring. The voltage dependence of this particular component of current is as exp(qV/nkT), where n is approximately 1.5. A fourth component, the surface current, stems from surface channels and varies with voltage as exp(qV/mkT), where m is usually between two and four for silicon junctions, although values larger than four have been noted for large channels[E7,E12,E13].

As was shown in the work by Goben and Smits[E9], neutron radiation of p-n junction devices produces a component of current which varies as exp(qV/nkT), where n is approximately 1.5 at room temperature and varies from 1.3 to 1.7 as the temperature ranges from 100°C to -50°C. This component of current is induced in the bulk transition region and dominates the transistor current gain over a wide range of current levels. These findings implies that emitter efficiency played a much more important role in radiation-induced changes in current gain than had been assumed in the past.

In 1949, Shockley[E10] pointed out that the injected minority carrier current in the base of a transistor depended on the ratio of the minority carrier mobility to the base doping, i.e., the sheet carrier density. Shockley further pointed out that, in the absence of collector multiplication, the collector current is simply the injected minority

carrier current modified by a recombination term, the base transport factor (base recombination term), which accounts for the carriers which recombine in the base region. The base current is composed of this recombination current, the space-charge recombination current, and the surface recombination current. Shockley then derived an expression for the current gain which ignored these fundamentally different currents.

Ignoring these different components of current apparently led previous researchers in the field of radiation behavior of transistor current gain to erroneous conclusions.

From Shockley's work, it may be seen that the best approach for studying the emitter efficiency in a p-n junction device is to ignore the simple expressions for emitter efficiency presented in the literature and instead study the emitter efficiency in terms of the components of current associated with the p-n junction.

Much work has been done on both permanent and transient radiation effects on semiconductor materials and semiconductor devices[E1]. A very small amount has involved detailed examination of the degradation of transistor current gain[E2-E6]. Most of the investigations have centered on characterizing parameters at particular bias conditions[E14-E23], or in measuring the effects of radiation on bulk semiconductor materials.

Transient radiation effects in semiconductor materials and devices are associated with the creation, by ionization,

of excess hole-electron pairs. Transient radiation effects disappear after the exciting radiation is removed in times on the order of the minority carrier lifetime. Permanent radiation effects are associated with damage to the lattice, whether or not the damage anneals out with time and temperature. Sander[E23] has recently shown that significant annealing is completed in times of the order of tens of seconds after the irradiation is stopped. Hood[E25] found the remaining damage to be stable at room temperature with less than a three per cent change in 3,000 hours although recent studies[E26] indicate a somewhat larger change. The permanent damage with which this research is concerned is the room temperature stable permanent damage.

Crystal lattice defects caused by radiation damage act as recombination sites and hence decrease the minority carrier lifetime. Crystal lattice defects, through impurity scattering and compensation of shallow impurities, reduce the carrier mobilities and the carrier concentration. Fast-neutron irradiation is particularly damaging to crystal lattices because thousands of atoms may be removed from their lattice sites as the result of a single collision[E24].

Loferski[E2], in the first investigation (1958) of transistor current gain degradation, employed the simple expression[E27-E32] for emitter efficiency involving only the ratios of the sheet resistivities of the base and emitter regions[E33,E34]. He concluded that the emitter efficiency would be negligible. By using a linear dependence of the

reciprocal lifetime on neutron fluence, Loferski modified Webster's equation[E28] to include fluence and concluded that the reciprocal of the common-emitter current gain should vary linearly with fluence. Discrepancies between theory and experiment were attributed to experimental error and the use of incorrect values for the constants in his theoretical expression.

Messenger and Spratt[E3], in their analysis (1959) of transistor gain degradation caused by neutron bombardment, again assumed the emitter efficiency to be essentially independent of neutron fluence. The theoretical analysis consisted of applying Shockley-Read[E35,E36] statistics to Webster's equation. From this analysis, Messenger and Spratt were able to calculate the energy of an assumed single level for the recombination sites. The recombination sites were assumed to be in the bulk base region and to act only through lifetime degradation. Cross-sections for interaction with the mobile carrier were also calculated. Discrepancies between theoretical and experimental results were attributed to lack of precise knowledge of the lifetime damage constant and to experimental error.

Easley and Dooley[E4] (1960) assumed the emitter efficiency to be independent of neutron flux, and further assumed that the emitter efficiency and collector multipication factor were equal to unity. Thus, the common-base current gain reflected only the base transport factor (base recombination term). The expression[E27-E32] for the base

recombination term was modified to exhibit a dependence on neutron flux by assuming a flux dependent lifetime and an electrical base width that varied with irradiation resulting from change in the carrier concentration. The expression which Easley and Dooley derived simplified to a linear dependence on flux for the assumption of fluxes too low to cause appreciable carrier removal. Experiments to verify the theory were carried out in a steady state reactor, with measurements made in-core. Disagreements were attributed to partial annealing of the radiation damage during bombardment.

In a later analysis (1964) of neutron degradation of transistor current gain, Hood[E5] allowed the emitter efficiency to vary with neutron fluence by the inclusion of the back-injection current term and a simplified form of the Sah-Noyce-Shockley[E12] expression for the normal bulk space-charge recombination-generation current term. The back injection into the emitter is normally negligible because of the high doping in the emitter, and the normal bulk space-charge recombination current is negligible at emitter-base biases greater than 0.3 volts. The discrepancy between Hood's theoretical and experimental results was greatest, where it would be expected to be the least, at low current levels. The discrepancy was attributed to neglecting the collector leakage current in his analysis.

In 1964, Goben[E9,E37] reported a base current with a voltage dependence of $\exp(qV/nkT)$, $n \approx 1.5$, which was

observed to increase in proportion to neutron fluence upon exposure to neutron radiation. From a study of the base resistance through which this current component flows, Goben[E9,E37] showed that this component is of bulk and not of perimeter origin and must be attributed to recombination in the bulk space-charge region. This current component dominates transistor gain over a wide range of current density and is primarily responsible for degradation of transistor current gain by decreasing the emitter efficiency. Goben[E38], in the analyses of the deviation of the characteristics from an exponential caused by the emission concentration in "ring-dot" structures and the transverse bias dependence of the base current components for a special "tetrode-type" test structure, found that the small "1.5 component" of current initially present is indeed of surface-perimeter origin while the added "1.5 component" of current induced by neutron bombardment is of bulk space-charge origin. An investigation was made of many different types of silicon transistors, and all were found to exhibit a similar neutron-induced component. In this work, Goben[E38] also found an apparent difference in annealing rates for the neutral base region and the space-charge region of the emitter-base junction.

Recent work by Goben et al.[E39] indicated, from a study of base and collector current as a function of the emitter-to-base voltage, that the neutron-induced base current had components originating in the emitter space-charge region as

well as the neutral base region. At low injection levels the neutron-induced base current was dominated by the space-charge component, whereas the high injection behavior appeared to be controlled by recombination in the neutral base region. Additional experiments performed in special tetrode transistor and van der Pauw-type sample indicated that changes in collector current were dominated by recombination in the neutral base, while changes in base doping and mobility had only a secondary effect. These conclusions were reached from experiments on transistors with a ring emitter, on tetrode-type test transistors, and on special Hall-effect devices.

Chott and Goben[E40] in a recent study (1967) found indications that the origin of the anomalous annealing was one, or a combination, of the following mechanisms: a quasi-tunneling recombination phenomena in the emitter-base space-charge region, or a dependence of the neutron-induced defect centers on the p-n junction field. A field dependence appeared to be present, but it was not certain whether the quasi-tunneling phenomena occurred, although it was shown that it is possible for such phenomena to occur. The annealing characteristics of the defects causing changes in the collector and base currents were obtained. Three sets of devices were irradiated and then annealed, with one set having a forward bias during annealing, one set having no bias, and one set having a reverse bias. The dependence of the field on annealing was present but appeared quite

complex. The presence of the externally applied field during annealing appeared to enhance the annealing of neutron-induced defects regardless of whether the junction was forward or reverse biased.

While studying the transient annealing effects in semiconductor devices, Sander and Gregory[E41] recently discovered that p-type material is very sensitive to the minority carrier injection level and the room temperature annealing rate can be increased by the presence of minority carriers. The injection dependence of n-type material is very small and is in the opposite sense (i.e., the room temperature annealing rate can be decreased by the presence of minority carriers). This behavior can be correlated on the basis of the hole-to-electron ratios of the different material types and resistivity.

Bass[E42] in his recent work of neutron damage and annealing in silicon found the carrier removal rate and the annealing behavior of n-type semiconductor to depend on the crystal-growth method. A slight dependence on the dopant impurity was observed in vacuum-float-zone material, but carrier removal in p-type semiconductor was not influenced by the growth method of the dopant impurity.

Curtis and Germano[E43] recently investigated the dependence of carrier lifetime on excess carrier density for bulk n-type and p-type silicon materials. Their results showed that the lifetime was constant at low excess densities, increased to a value several times larger at excess densities

near the equilibrium carrier density, and then decreased. In fitting the model for lifetime versus excess carrier, an activation energy of 0.32eV above the valence band or 0.35eV below the conduction band was found to give the best fit.

Curtis[E44] concluded that recombination was dominated by sites within defect clusters, and that there was no dependence on oxygen concentration or type of defect in n-type material. A very small dependence on dopant was noted in heavily doped p-type material. It was also concluded that it was impossible to fit all the experimental data with a single level recombination model. A two level model for recombination processes in neutron irradiated materials and devices was proposed by Messenger[E45]. This model successfully explained the previously published experimental data for lifetime, lifetime damage constant as a function of resistivity, lifetime damage constant as a function of injection level and temperature. Two deficiencies in Messenger's model should be noted: 1) the two level model is an approximation to a very complicated defect structure which is known to contain many levels; 2) there are several plausible alternative extensions and modifications to the one level model which might also resolve its contradictions with the experimental data.

A computer program was written by Gwyn, Scharfetter and Wirth[E46] for the prediction of transient and permanent radiation damage in p-n junction devices. The program automatically solved the Poisson's equation and the continuity

equations over a one-dimensional region. It included non-linear mobility, lifetime and the Shockley-Read-Hall recombination statistical model[E12,E35]. The program should predict the electrical properties of a defect state with considerable accuracy.

Frank and Taulbee[E26] in their recent study of transistor current gain prediction after neutron irradiation found that carrier injection and elevated temperatures in normally biased transistors can produce 20-25 percent less measured damage than in passively irradiated devices. Room temperature annealing[E46] was found to be 15-20 percent over a period of several weeks whereas high carrier injection[E26] was found to produce a temporary 10-15 percent increase in damage. Their work[E26] also shows that silicon junction capacitance at low voltage is frequency dependent after large neutron exposures.

The accumulation of positive charge[E47] has been reported previously as the dominant mechanism responsible for the surface effect in oxide passivated devices. The existence of the positive charge effect and the introduction of acceptor-like surface recombination states has been demonstrated by Maier[E48] recently, and the additional surface recombination states[E48] are shown to be the dominant mechanism for the surface effect in oxide passivated devices.

REFERENCES

E1. "The Effect of Nuclear Radiation on Semiconductor Devices," Batelle Memorial Institute, Radiation Effects Information Center (Columbus, Ohio) REIC Report No. 10, April 30, 1960, and Addendum, July 15, 1961.

E2. Loferski, J. K., "Analysis of the Effect of Nuclear Radiation on Transistors," J. Appl. Phys., 29: 35-40, 1958.

E3. Messenger, G. C. and Spratt, J. P., "The Effects of Neutron Irradiation on Germanium and Silicon," Proc. IRE, 46: 1038-1044, 1958.

E4. Easley, J. W. and Dooley, J. A., "On the Neutron Bombardment Reduction of Transistor Current Gain," J. Appl. Phys., 31: 1024-1028, 1960

E5. Hood, J. A., "Predicting the Current Gain Degradation in n-p-n Silicon Transistors after Irradiation by High-Energy Neutrons," Sandia Lab. (Albuquerque, N. M.) (Publication) SC-TM-64-69, 1964.

E6. Easley, J. W., "Radiation Damage to Semiconductor Devices," Sandia Lab. (Albuquerque, N. M.) (Publication) SCR-532, 1962.

E7. Iversen, J. W., Bray, A. R. and Kleinmack, J. J., "Low-Current Alpha in Silicon Transistors," IRE Trans. on Electron Devices, ED-9: 474-478, 1962.

E8. Coppen, P. J. and Matzen, W. T., "Distribution of Recombination Current in Emitter-Base Junctions of Silicon Transistors," IRE Trans. on Electron Devices, ED-9: 75-81, 1962.

E9. Goben, C. A. and Smits, F. M., "Anomalous Base Component in Neutron Irradiated Transistors," IEEE Radiation Effects Conference, Seattle, Washington, 1964.

E10. Shockley, W., "The Theory of p-n Junctions in Semiconductors and p-n Junction Devices," Bell System Tech. J., 38: 435-589, 1949.

E11. Moll, J. L. and Ross, L. M., "The Dependence of Transistor Parameters on the Distribution of Base Layer Resistivity," Proc. IRE, 44: 72-76, 1956.

E12. Sah, C. T., Noyce, R. N. and Shockley, W., "Carrier Generation and Recombination in p-n Junctions and p-n Junction Characteristics," Proc. IRE, 45: 1228-1243, 1957.

E13. Sah, C. T., "Effect of Recombination and Channel on p-n Junction and Transistor Characteristics," IRE Trans. on Electron Devices, ED-9: 94-108, 1962.

E14. DeNure, D. G., "Effect of Fast Neutron Bombardment on Type 2N559 and 2N559E Epitaxial p-n-p Germanium Switching Transistors," Bell Telephone Lab. (Murray Hill, N. J.) (Publication) MM-61-4252-33, 1961.

E15. Hood, J. A., "Degradation of n-p-n Silicon Planar Transistors with Bombardment by High-Energy Neutron," Sandia Lab. (Albuquerque, N. M.) (Publication) SC-TM-261-73(14), 1963.

E16. Hood, J. A., "Neutron-Induced Degradation of Commercial Transistors," Sandia Lab. (Albuquerque, N. M.) (Publication) SC-TM-129-63(14), 1963.

E17. Westmark, C. I. and Rice, W. H., "Radiation-Induced Degradation of DC Current Gain and Collector-To-Emitter Saturation Voltage for Selected Power Transistors," Sandia Lab. (Albuquerque, N. M.) (Publication) SC-TM-223-63(14), 1963.

E18. Sanders, H. H., "Neutron Permanent Damage Data for the 2N1675 Transistor," Sandia Lab. (Albuquerque, N. M.) (Publication) SC-RR-65-550, 1964.

E19. Manlief, S. K., "A Method of Measuring the Minority Carrier Base Transit Time in a Junction Transistor Exposed to a Neutron Environment," Sandia Lab. (Albuquerque, N. M.) (Publication) SC-TM-314-63(14), 1963.

E20. Levy, G. F., Fouse, R. R. and Castner, S. V., "The Effects of Nuclear Radiation on Some Selected Semiconductor Devices," Proc, of the 2nd Conf. on Nuclear Radiation Effects on Semiconductor Devices, Materials and Circuits, 76-81, 1959

E21. Loferski, J. J., "A Brief Resume of Radiation Effects on Semiconductor Materials and Devices," Proc. of the 2nd Conf. on Nuclear Radiation Effects on Semiconductor Devices, Materials and Circuits, 8-10, 1959.

E22. Smits, F. M., "On the Energy Dependence of Neutron Damage to Silicon Transistors," Sandia Lab. (Albuquerque, N. M.) (Publication) SC-R-64-196, 1964.

E23. Sander, H. H., "Room Temperature Annealing of Silicon Transistor Parameters Degraded by a Burst of Neutrons," Sandia Lab. (Albuquerque, N. M.) (Publication) SC-R-64-192, 1964.

E24. Billington, D. S. and Crawford, J. H., Jr., Radiation Damage in Solids, Princeton, N. J., Princeton University Press, 1961.

E25. Hood, J. A., "Predicting the Current Gain Degradation in n-p-n Silicon Transistors after Irradiation by High-Energy Neutrons," Sandia Lab. (Albuquerque, N. M.) (Publication) SC-TM-64-69, 1964.

E26. Frank, M. and Taulbee, C. D., "Factors Influencing Prediction of Transistor Current Gain in Neutron Radiation," IEEE Trans. on Nuclear Science, NS-14: 6, 127-133, 1967.

E27. Shockley, W., "The Theory of p-n Junctions in Semiconductors and p-n Junction Devices," Bell System Tech. J., 28: 435-589, 1949.

E28. Webster, W. M., "On the Variation of Junction-Transistor Current-Amplification Factor with Emitter Current," Proc. IRE, 42: 914-920, 1954.

E29. Rittner, E. S., "Extension of the Theory of the Junction Transistor," Phys. Rev., 94: 1161-1171, 1954.

E30. Fletcher, N. H., Note on, "The Variation of Junction Transistor Current-Amplification Factor with Emitter Current," Proc. IRE, 44: 1475-1476, 1956.

E31. Matz, A. W., "Variation of Junction Transistor Current Amplification Factor with Emitter Current," Proc. IRE, 46: 616-617, 1958.

E32. Jakits, O. H., "Some Comments on Webster's Equation," IEEE Trans. on Electron Devices, ED-10: 292-294, 1962.

E33. Tanenbaum, M. and Thomas, D. E., "Diffused Emitter and Base Silicon Transistors," Bell System Tech. J., 35: 1-22, 1956.

E34. Boothroyd, A. R. and Trofimenkoff, F. N., "Determination of the Physical Parameters of Transistors of Single and Double-Diffused Structure," IEEE Trans. on Electron Devices, ED-10: 149-163, 1963.

E35. Shockley, W. and Read, W. T., Jr., "Statistics of the Recombinations of Holes and Electrons," Phys. Rev., 87: 835-842, 1952.

E36. Shockley, W., "Electrons, Holes and Traps," Proc. IRE, 46: 973-990, 1958.

E37. Goben, C. A., "Neutron Bombardment Reduction of

Transistor Current Gain," Ph.D. Thesis, Iowa State University Library, Ames, Iowa, 1965.

E38. Goben, C. A., "A Study of the Neutron-Induced Base Current Component in Silicon Transistors," IEEE Radiation Effects Conference, Ann Arbor, Michigan, 1965. IEEE Trans. on Nuclear Science, NS-12: 5. 134-146, 1965.

E39. Goben, C. A., Smits, F. M. and Wirth, J. L., "Neutron Radiation Damage in Silicon Transistors," IEEE Trans. on Nuclear Science, to be published April, 1968.

E40. Chott, J. R. and Goben, C. A., "Annealing Characteristics of Neutron Irradiation Silicon Transistors," IEEE Trans. on Nuclear Science, NS-14: 6, 134-146, 1967.

E41. Sander, H. H. and Gregory, B. L., "Transient Annealing in Semiconductor Devices Following Pulsed Neutron Irradiation," IEEE Trans. on Nuclear Science, NS-13: 6, 53-62, 1966.

E42. Bass, R. F., "Influence of Impurities on Carrier Removal and Annealing in Neutron-Irradiated Silicon," IEEE Trans. on Nuclear Science, NS-14: 6, 78-81, 1967.

E43. Curtis, O. L., Jr. and Germano, C. A., "Injection-Level Studies in Neutron-Irradiated Silicon," IEEE Trans. on Nuclear Science, NS-14: 6, 68-77, 1967.

E44. Curtis, O. L., Jr., "Effects of Oxygen and Dopant on Lifetime in Neutron-Irradiated Silicon," IEEE Trans. on Nuclear Science, NS-13: 6, 33-40, 1966.

E45. Messenger, G. C., "A Two Level Model for Lifetime Reduction Processes in Neutron Irradiated Silicon and Germanium," IEEE Trans. on Nuclear Science, NS-14: 6, 88-102, 1967.

E46. Gwyn, C. W., Scharfetter, D. L. and Wirth, J. L. "The Analysis of Radiation Effects in Semiconductor Junction Devices," IEEE Trans. on Nuclear Science, NS-14: 6, 153-169, 1967.

E47. Hughes, H. L., "Comparative Study of Ionizing Radiation Surface Effects, Utilizing MOS Device Fabricated with Various Dielectrics," IEEE Annual Conference on Nuclear and Space Radiation Effects, Palo Alto, Calif., July, 1966.

E48. Maier, R. J., "Radiation Induced Surface Recombination in Oxide Passivated Transistors," IEEE Trans. on Nuclear Science, NS-14: 6, 252-259, 1967.

APPENDIX F: BACKGROUND OF THE PROBLEM

An anomalous neutron-induced base current component has been identified[F1,F2] and found to vary with voltage[F3] as

$$I_{B_{INC}} = K_V \cdot x_m(V_{BE}) \cdot A_E \cdot \phi \cdot \exp(qV_{BE}/nkT) \quad \text{(F-1)}$$

where $x_m(V_{BE})$ = depletion layer width (cm),

A_E = deffective emitter area (cm^2),

K_V = damage constant (amperes/cm^3/nvt),

ϕ = neutron fluence (nvt),

$n \simeq 1.5$.

This neutron-induced base current increases in proportion to the neutron fluence as indicated in equation (F-1). It was found to dominate the transistor current gain over a wide range of current levels and to be primarily responsible for the degradation of current gain at low and intermediate current levels through degradation of the emitter efficiency.

Anomalous annealing phenomena, which have also been studied previously[F1-F4], indicate that the neutron-induced defects in the emitter-base space-charge region of a transistor anneal differently from defects in the neutral base region. A recent study has found indications that the origin of the anomalous annealing was one, or a combination, of the following mechanisms[F5]: a quasi-tunneling recombination phenomena in the emitter-base space-charge region, or a dependence of the neutron-induced defect centers on the p-n junction field. A slight field dependence in the anomalous annealing of neutron-induced defects was also observed

recently but appeared to be quite complex[F5]. This unsolved problem of the field dependence in the anomalous annealing of neutron-induced defects has to be further investigated.

It was pointed out that as the applied bias increases from 0.1 volt to 1.0 volt, the depletion layer width and, hence, volume changed only by a factor of three while the term exp(qV/nkT) changed by about 30,000,000. The unsolved question of the anomalous annealing of neutron-induced defects may be due to the narrow depletion layer width of the emitter-base junction.

Impurity profiles[F6] of 2N914 transistors indicate that the depletion layer width of the collector-base junction is about 5 times wider than that of the emitter-base junction. The effective area of the collector-base junction is 5.39 times greater than that of the emitter-base junction.

If the roles of the collector and emitter are interchanged (i.e., with the normal emitter operated as a "collector" and the normal collector operated as an "emitter" and the base remaining unchanged) the bulk space-charge region of the new "emitter-base" junction is about 26.5 times that of the normal emitter-base junction. This makes it easier to study the neutron-induced base current which had been found to depend on the bulk space-charge region and to study the field dependence in the anomalous annealing of the neutron-induced defects.

Much work has been done on surface effects in semiconductor material and semiconductor devices[F7-F11]. A very

small amount of work has involved examination of the surface effects on neutron bombarded devices[F12]. Surface effects in germanium devices with reverse bias applied to the junction during electron irradiation have been observed[F7]. Since the concentration of the emitter of 2N914 transistor is about 1.67×10^5 times that of the collector, the Fermi level in the emitter region is closer to the conduction band than is the Fermi level in the collector region. Thus, inversion layers are more easily formed in the "emitter-base" junction region when the devices are operated in the inverse configuration. This allows the study of the neutron-induced surface effects by operating the devices in the inverse configuration during irradiation.

The diffusion potential, V_T, for nondegenerate material at thermal equilibrium varies with the impurity concentration at both sides of the junction as[F8]:

$$V_T = \frac{kT}{q} \ln(N_A \cdot N_D / n_i^2), \qquad \text{(F-2)}$$

where N_A = hole concentration in the p-type semiconductor,

N_D = electron concentration in the n-type semiconductor,

n_i = intrinsic carrier concentration,

k = Boltzmann's constant (8.63×10^{-5} eV/°K),

T = absolute temperature in degrees Kelvin,

q = charge of electron (1.6×10^{-9} coulomb).

Since N_A and N_D change after neutron radiation, V_T changes

after neutron radiation. This suggests the study of the radiation and annealing effects of the diffusion potential (V_T).

The activation energy which characterizes the recovery of the defects can be calculated by a combination of isothermal and isochronal annealing data[F13] of two identical devices (see Appendix G).

In order to determine the effect of different biasing voltages on the activation energy in a certain temperature range, three sets of paired devices can be annealed, each pair annealed at a different junction bias voltage, one device of each pair used for isothermal annealing and the other device of each pair used for isochronal annealing. This also allows the study of the annealing rate of neutron-induced defects in the bulk space-charge region and in the neutral base region.

REFERENCES

F1. Goben, C. A. and Smits, F. M., "Anomalous Base Current Component in Neutron Irradiated Transistors," IEEE Radiation Effects Conference, Settle, Washington, 1964.

F2. Goben, C. A., "A Study of the Neutron-Induced Base Current Component in Silicon Transistors," IEEE Radiation Effects Conference, Ann Arbor, Michigan, 1965. IEEE Trans. on Nuclear Science, NS-12:.5, 134-146, 1965.

F3. Gassner, G. E., "Variation of Inverse Parameters with Neutron Radiation in Silicon Transistors," Unpublished M.S. Research, University of Missouri-Rolla, 1968.

F4. Goben, C. A., Smits, F. M. and Wirth, J. L., "Neutron Radiation Damage in Silicon Transistors," IEEE Trans. on Nuclear Science, to be published in April, 1968.

F5. Chott, J. R. and Goben, C. A., "Annealing Characteristics of Neutron Irradiated Silicon Transistors," IEEE Trnas. on Nuclear Science, NS-14: 6, 134-146, 1967.

F6. Chow, M. C., Unpublished Ph.D. Research, University of Missouri-Rolla, 1968.

F7. Baruch, P., "Mobility of Radiation-Induced Defects in Germanium," J. Appl. Phys., 32: 4, 653-659, 1961.

F8. Phillips, A. B., Transistor Engineering, McGraw-Hill New York, 86-91, 1962.

F9. Iwersen, J. W., Bray, A. R. and Kleinmack, J. J., "Low-Current Alpha in Silicon Transistors," IRE Trans. on Electron Devices, ED-9: 474-478, 1962.

F10. Sah, C. T., Noyce, R. N. and Shockley, W., "Carrier Generation and Recombination in p-n Junctions and p-n Junction Characteristics," Proc. IRE, 45: 1228-1243, 1957.

F11. Sah, C. T., "Effect of Recombination and Channel on p-n Junction and Transistor Characteristics," IRE Trans. on Electron Devices, ED-9: 94-108, 1962.

F12. Maier, R. J., "Radiation Induced Surface Recombination on Oxide Passivated Transistors," IEEE Trans. on Nuclear Science, NS-14: 6, 252-259, 1967.

F13. Meechan, E. J. and Brinkman, J. A., "Electrical Resistivity Study of Lattice Defects Introduced in Copper by 1.25-MeV Electron Irradiated at 80°K," Phys. Rev., 103: 5, 1193-1202, 1956.

APPENDIX G: ACTIVATION ENERGY DETERMINATION

The recovery of current component changes in transistors during annealing treatments is frequently observed to obey a rate equation of the form[G1]

$$\frac{dI}{dt} = F(I,q_1,q_2, \cdots q_n) \cdot \exp(-E_a/kT), \qquad (G-1)$$

where I represents either I_B or I_C in this work; t, the time; T, the absolute temperature; k, Boltzman's constant; and E_a, the activation energy for the recovery process. The q's represent other variables, independent of time (t) and temperature (T). They can be constant or a function of current (I) for devices having identical characteristics[G1].

In general, equation (G-1) can be integrated as follows:

$$\lambda(I,q_1,q_2, \cdots q_n) = \int_{I_o}^{I} \frac{dI}{F(I,q_1,q_2, \cdots q_n)} \qquad (G-2)$$

$$= \int_{o}^{t} \exp(-E_a/kT) \cdot dt$$

$$= \theta$$

where θ is the temperature-compensated time. For identical devices, the q's are either constant or a function of current and need not be considered. Then for any annealing run:

$$\Delta\theta_i = \theta_i - \theta_{i-1} = \Delta t \cdot \exp(-E_a/kT), \qquad (G-3)$$

where Δt is the total annealing time for the i^{th} annealing

run.

Considering only isochronal annealing, Δt is a constant denoted as M. If the recovery is characterized by a single activation energy, E_a, equation (G-3) can be written as:

$$\ln(\Delta\theta_i) = N_a - \frac{E_a}{kT_i}, \tag{G-4}$$

where $N_a = \ln(M)$, and T_i is the *ith* isochronal annealing temperature.

Considering isothermal annealing only, equation (G-2) can be expressed as:

$$\tau = \theta \cdot \exp(E_a/kT_a), \tag{G-5}$$

where T_a denotes a certain isothermal annealing temperature, and τ the annealing time.

Let τ_i denote the value of τ corresponding to θ_i. From equation (G-5) one obtains

$$\Delta\tau_i = \tau_i - \tau_{i-1} = \Delta\theta_i \cdot \exp(E_a/kT_a) \tag{G-6}$$

$$\ln(\Delta\tau_i) = \ln(\Delta\theta_i) + E_a/kT_a \tag{G-7}$$

From equation (G-4) and (G-7), one may obtain

$$\ln(\Delta\tau_i) = C - \frac{E_a}{kT_i}, \tag{G-8}$$

where $C = N_a + E/kT_a$.

Thus, the activation energy can be expressed as:

$$E_a = \frac{\ln(\Delta\tau_i/\Delta\tau_{i-1})}{(1/T_i - 1/T_{i-1})/k}$$

Using both isothermal and isochronal annealing data of I_B or I_C, the activation energy, E_a, which characterizes the annealing of defects in the space-charge region or in the neutral base region, respectively, can be calculated.

REFERENCE

G1. Meechan, E. J. and Brinkman, J. A., "Electrical Resistivity Study of Lattice Defects Introduced in Copper by 1.25-MeV Electron Irradiated at 80°K," Phys. Rev., 103: 5, 1193-1202, 1956.

APPENDIX H: ERROR ANALYSES OF THE ANNEALING DATA AND OF THE ACTIVATION ENERGY CALCULATIONS

1. Error Calculation of the Annealing Factor (AF)

As stated in Appendix A, the Automatic Data Acquisition System[H1] is capable of measuring current and voltage with an overall absolute accuracy of ±1%. If the computer error is neglected, then the maximum error of I_B and I_C used in this work should be ±1%. Thus, errors in the annealing factor (AF) based on errors of I_B or I_C can be calculated.

The annealing factor of defects in the space-charge region is defined by:

$$AF = \frac{I_B(\phi,t) - I_B(0,0)}{I_B(\phi,0) - I_B(0,0)} \qquad \text{(H-1)}$$

where AF is the annealing factor neglecting any error. $I_B(\phi,t)$ is I_B after annealing, $I_B(\phi,0)$ is I_B after irradiation, and $I_B(0,0)$ is I_B pre-irradiation. If the errors in I_B are included the annealing factor with error correction, AF_R, should be, for worst case:

$$AF_R = \frac{[I_B(\phi,t) - I_B(0,0)](1 \pm 0.02)}{[I_B(\phi,0) - I_B(0,0)](1 \pm 0.02)} \qquad \text{(H-2)}$$

Since $0.02 \ll 1$,

$$AF_R \simeq AF(1 \pm 0.02) \cdot (1 \pm 0.02)$$

$$AF_R \simeq AF(1 \pm 0.04) \qquad \text{(H-3)}$$

Similarly, the annealing factor of defects in the neutral base region should be AF(1 ± 0.04). Therefore, the annealing data in this work differ by less than 4% in most cases.

2. Error Calculation of the Activation Energy (E_a)

As shown in Appendix G, the activation energy (E_a) can be expressed by combining the isothermal and isochronal annealing data as:

$$E_a = - \frac{\ln(\Delta\tau_i/\Delta\tau_{i-1})}{(1/T_i - 1/T_{i-1})/k} , \qquad \text{(H-4)}$$

where T_i = the *ith* isochronal annealing temperature,

τ_i = the isothermal annealing time corresponding to T_i.

The errors of the annealing time ($\Delta\tau_i$) used in this work are less than ±10% while errors in the annealing temperature (T_i) have been found to be less than 1%. Thus, errors in the activation energy based on errors in the annealing time can be calculated.

If the errors in $\Delta\tau_i$ are included, the activation energy with error correction (E_{aR}) should be, for worst case:

$$E_{aR} = - \frac{\ln[\Delta\tau_i(1 \pm 0.1)/\Delta\tau_{i-1}(1 \pm 0.1)]}{(1/T_i - 1/T_{i-1})/k} . \qquad \text{(H-5)}$$

Thus, E_{aR} has maximum error when alternative signs are chosen in the numerator and denominator of the logarithm term. Using the (+) sign in the numerator and the (-) sign

in the denominator, equation (H-5) becomes

$$E_{aR} \simeq E_a \frac{\ln(\Delta\tau_i/\Delta\tau_{i-1})(1 + 0.22)}{\ln(\Delta\tau_i/\Delta\tau_{i-1})} . \qquad (H-6)$$

Using the (-) sign in the numerator and (+) sign in the denominator, equation (H-5) becomes

$$E_{aR} \simeq E_a \frac{\ln(\Delta\tau_i/\Delta\tau_{i-1})(1 - 0.18)}{\ln(\Delta\tau_i/\Delta\tau_{i-1})} . \qquad (H-7)$$

Since $\Delta\tau_i/\Delta\tau_{i-1} < 3$ for the annealing data used in this work, equation (H-6) and equation (H-7) can be expressed as:

$$E_{aR} \simeq E_a(1 \pm 0.18). \qquad (H-8)$$

Therefore, the activation energy calculated in this work differ by less than 18% in most cases.

Other sources of error have been found to be much less than 1% as cited.